

QOQAE

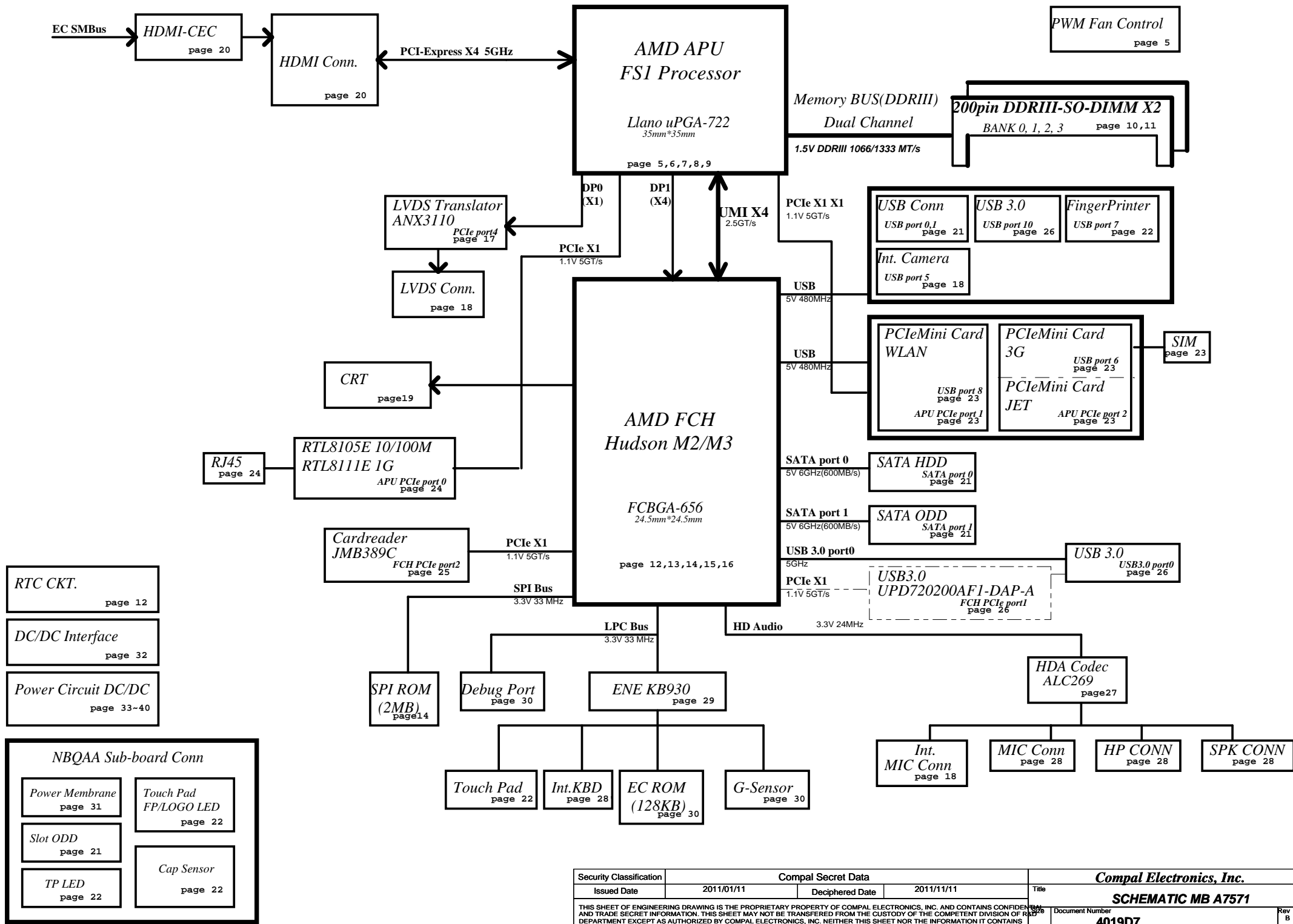
Ontario 10AS

LA-7571P REV 1.0 Schematic

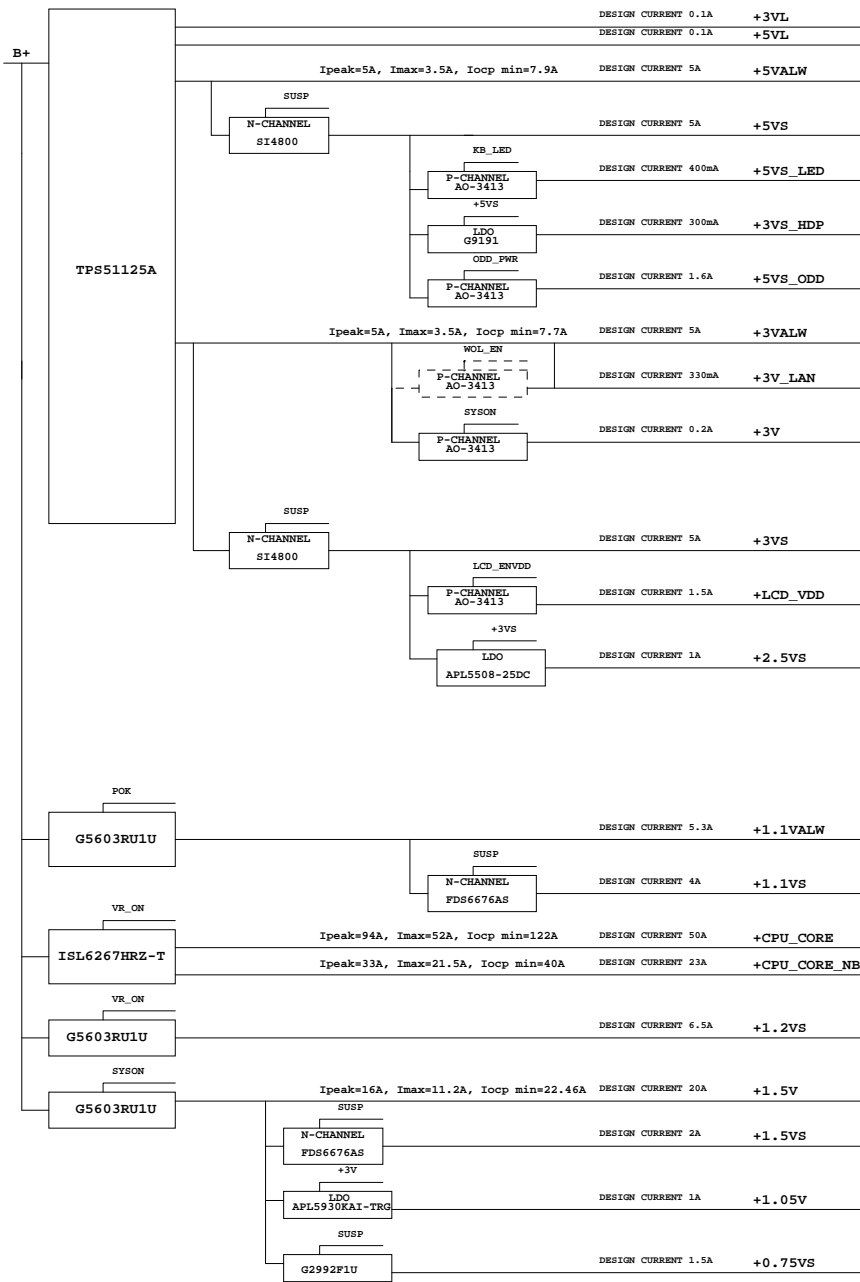
AMD Llano FS1 Processor / Hudson M2/M3

2011-05-04 Rev 1.0

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				Document Number	
				4019D7	
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Voltage Rails (O MEANS ON X MEANS OFF)

<div>power plane</div> <div>State</div>	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +1.1VALW +VSB	+1.5V +3V +1.05V	+5VS +3VS +2.5VS +1.5VS +1.2VS +1.1VS +0.75VS +CPU_CORE +CPU_CORE_NB
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

BTO Option Table

Function	HDMI-CEC		LAN		CAM+MIC	KB LED	Renesas USB3.0
description		Y	U	V	X	K	Reserved
explain	HDMI	HDMI+CEC	10/100	10/100/1000	CAM	KB LED	Renesas USB3.0
BTO		CEC@	8105E@	8111E@	CAM@	KBL@	RENE@

Function	ODD		Mini Card		Chipset		EC	
description		T	G	J	3G/JET	FCH	N/A	Reserved
explain	Normal	Slot	3G	JET		Hudson-M3	KB-930	KB-9012
BTO	ODD0@	ODD1@	3G@	JET@	3GJET@	HUDM3R1@ HUDM3R3@	KB930@	KB9012@

Function	FCH		UMA	
description	HM2	HM3	UM	
explain	Hudson-M2	Hudson-M3		
BTO	M2@	M3@		

STATE \ SIGNAL	SLP_S3#	SLP_S5#
Full ON	HIGH	HIGH
S1(Power On Suspend)	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH
S4 (Suspend to Disk)	LOW	HIGH
S5 (Soft OFF)	LOW	LOW
G3	LOW	LOW

FCH SM Bus Address (SCL0/SDA0)

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	WLAN		
+3VS	3G		

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b
+3VL	HDMI-CEC	34 H	0011 0100 b
Power	Device	HEX	Address
+3VL	Cap. Sensor		Virtual I2C

EC SM Bus2 Address

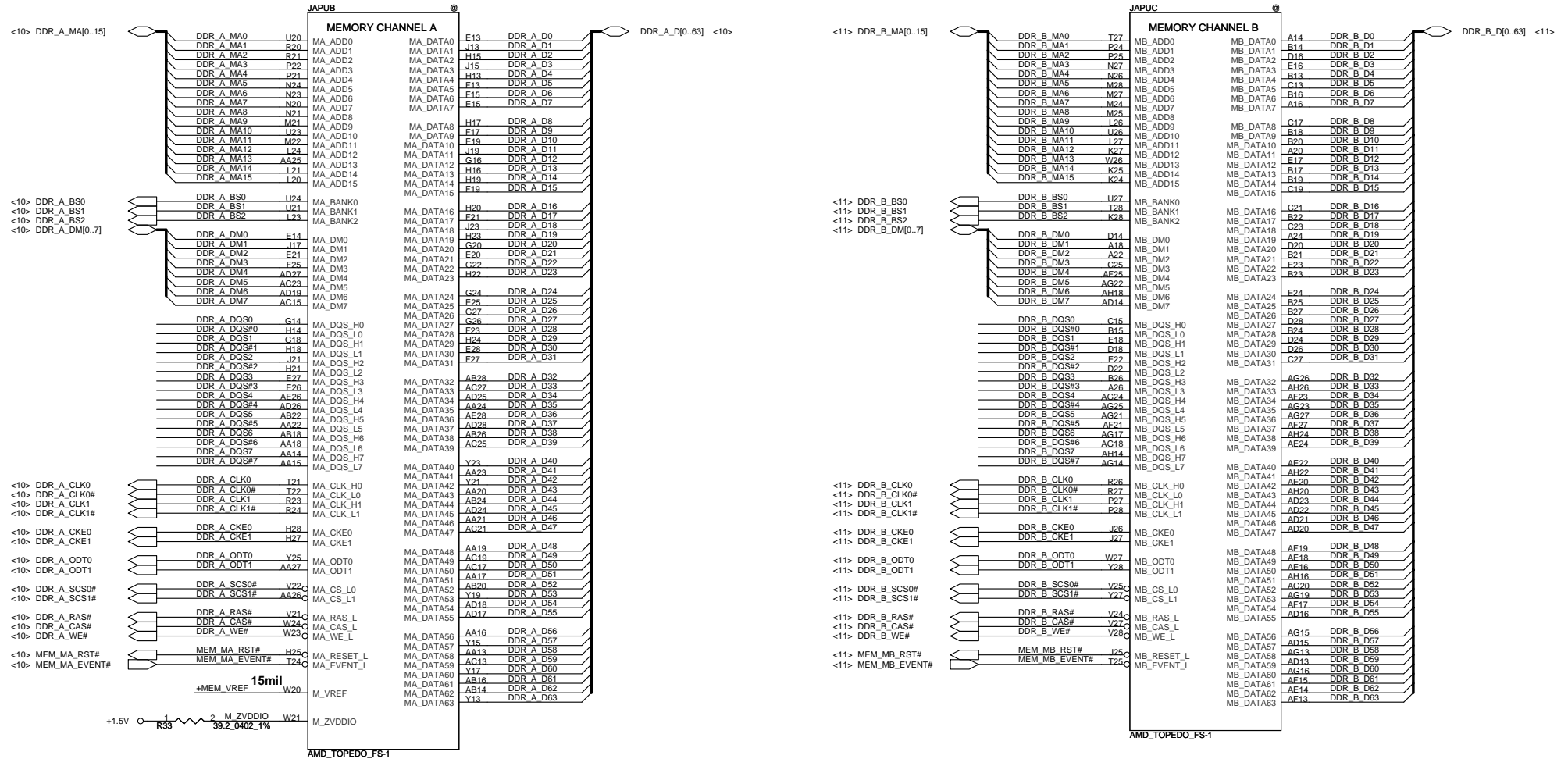
Power	Device	HEX	Address
+3VS	G-Sensor	40 H	0100 0000 b

<10> DDR_A_DQS[0..7]

<10> DDR_A_DQS# [0..7]

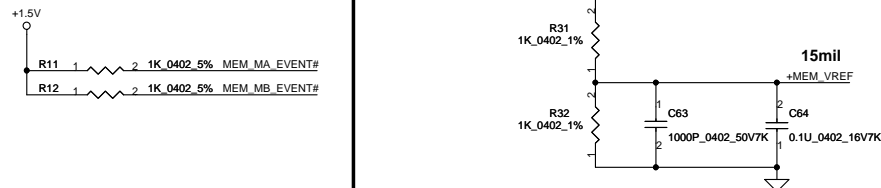
<11> DDR_B_DQS[0..7]

<11> DDR_B_DQS# [0..7]



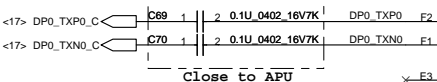
EVENT# pull high

0.75V Reference Voltage

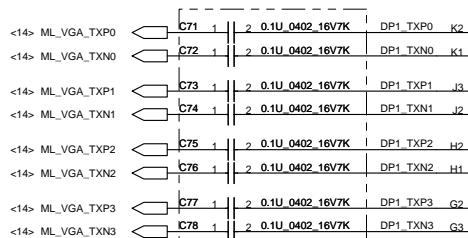


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To LVDS Translator

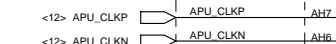


Close to APU

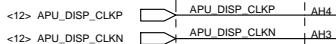


To FCH

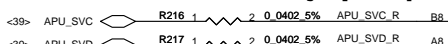
100MHz (SS)



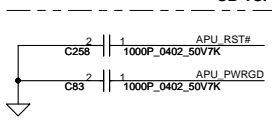
100MHz (NSS)



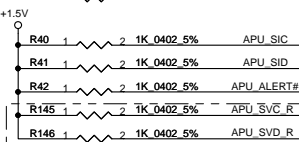
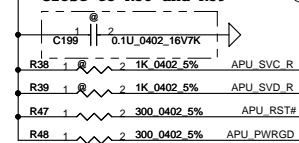
route on high speed layer



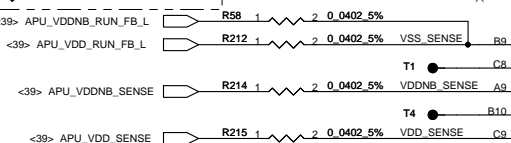
SB-TSI



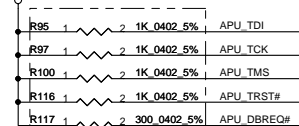
Close to R38 and R39



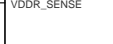
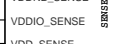
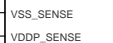
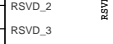
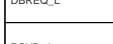
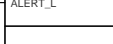
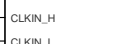
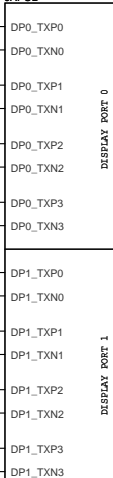
Avoid leakage issue



Close to JHDT

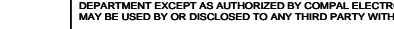
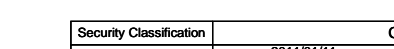
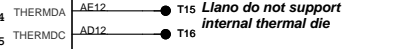
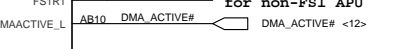
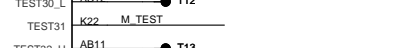
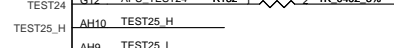
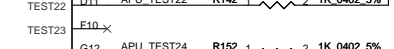
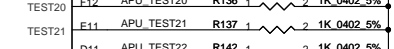
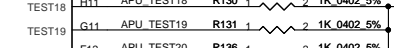
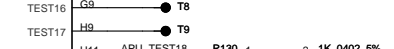
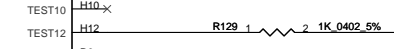
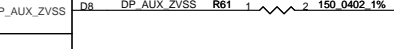
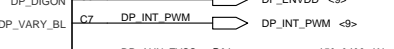
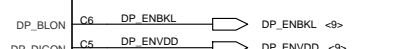
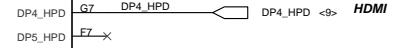
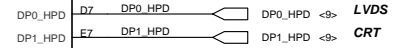
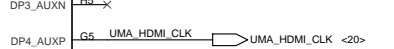
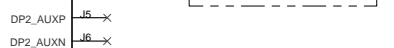
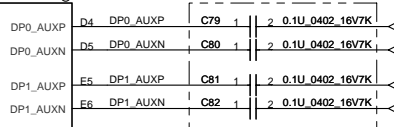


JAPU



AMD_TOPEDO_FS-1

Close to APU

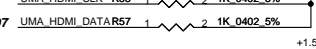
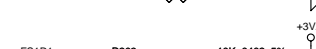
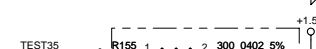
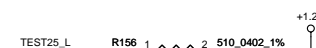
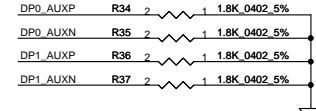


To LVDS Translator

To FCH

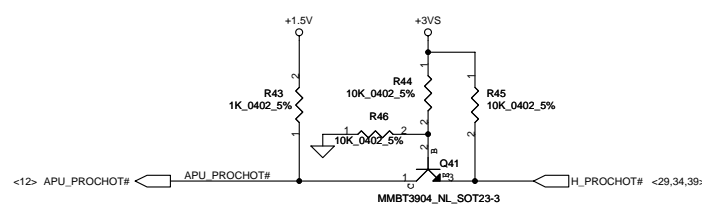
AUX 2~5 are for GFX interface use, they could be selected to DDC or AUX logic

VDDIO level
Need level shifter

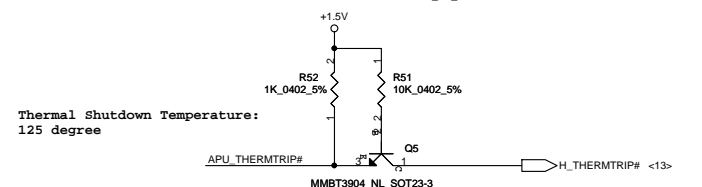


design guide 2K PH P.97

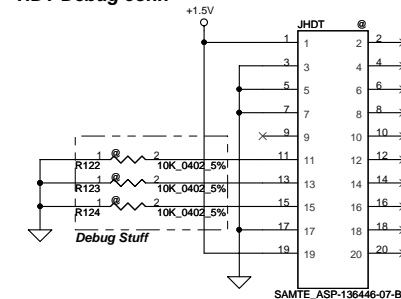
Avoid leakage issue



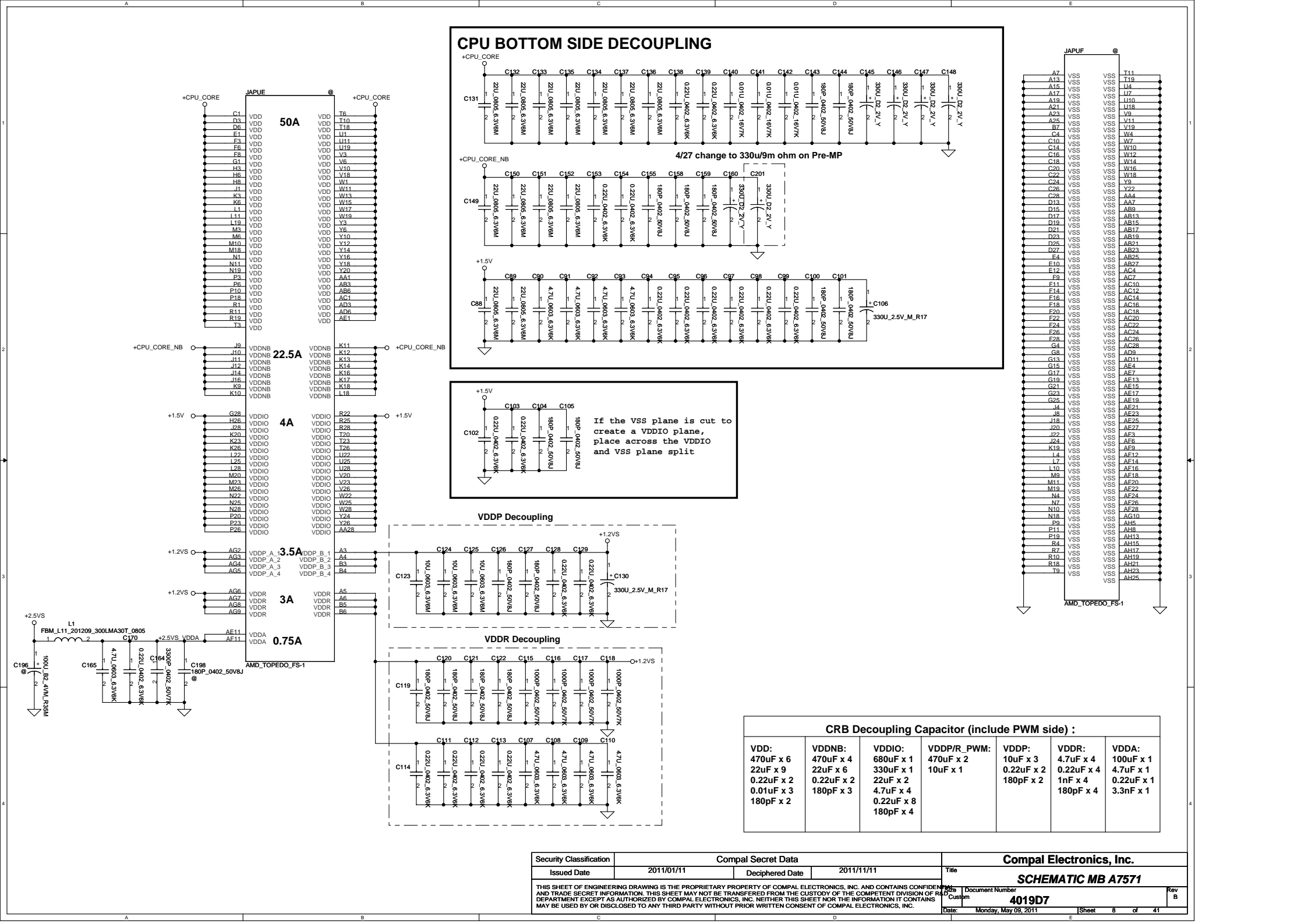
Thermal Shutdown Temperature:
125 degree



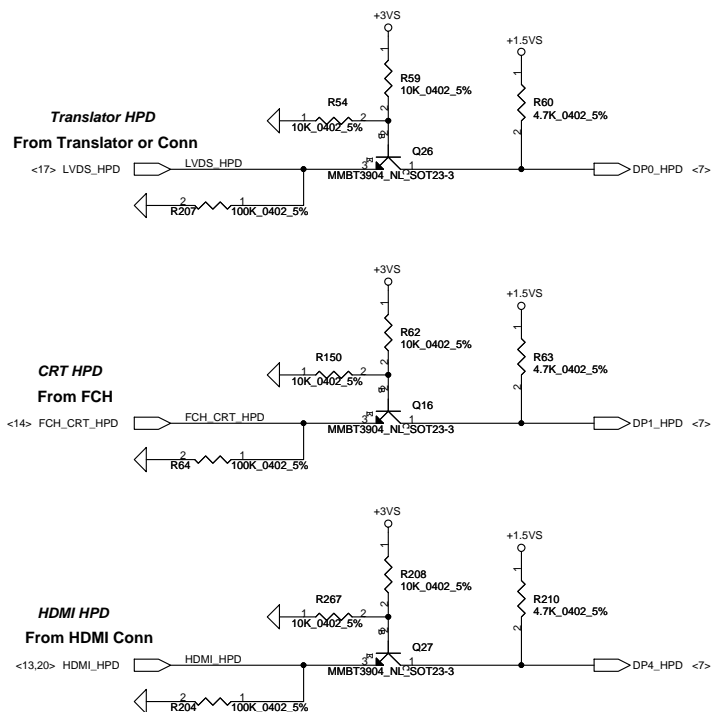
HDT Debug conn



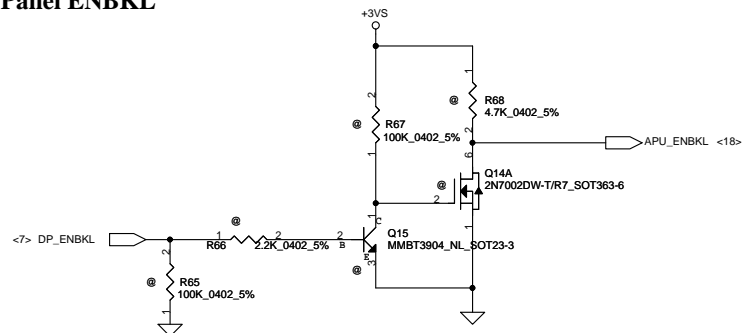
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					Date:	Monday, May 09, 2011



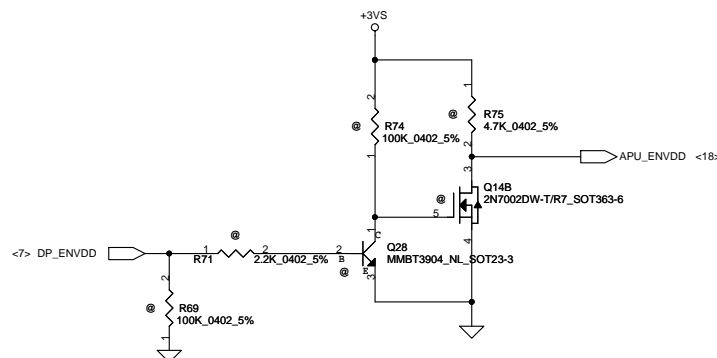
HPD



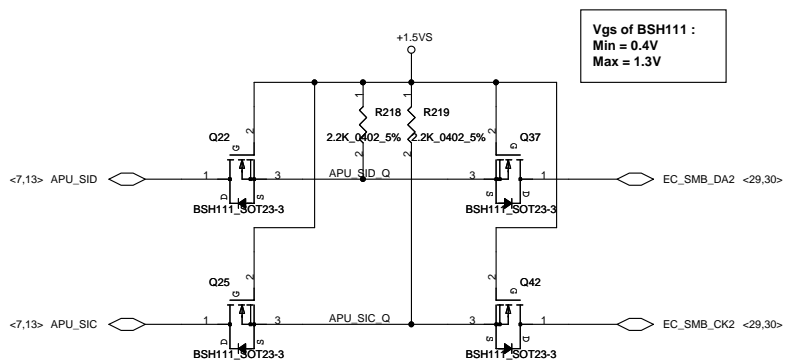
Panel ENBKL



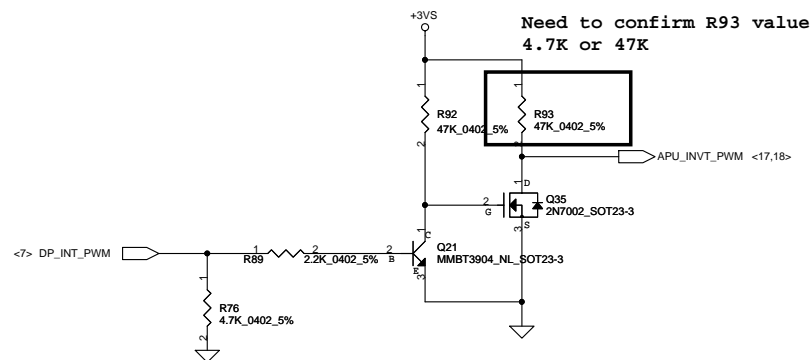
Panel ENVDD



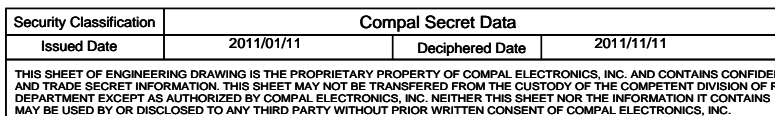
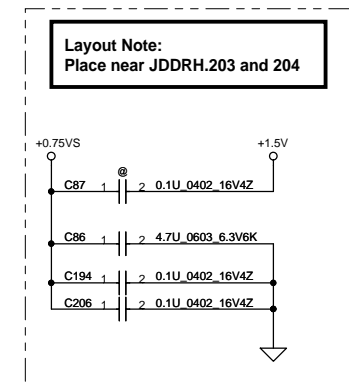
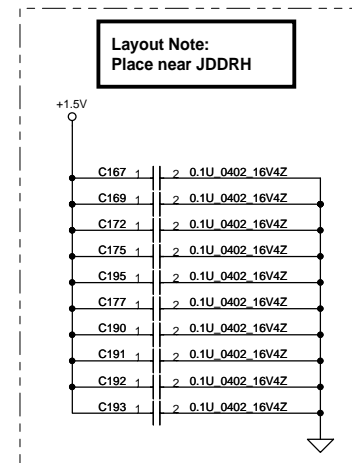
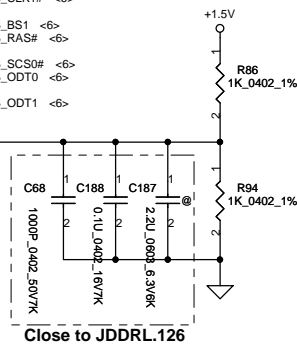
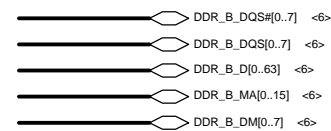
SB-TSI



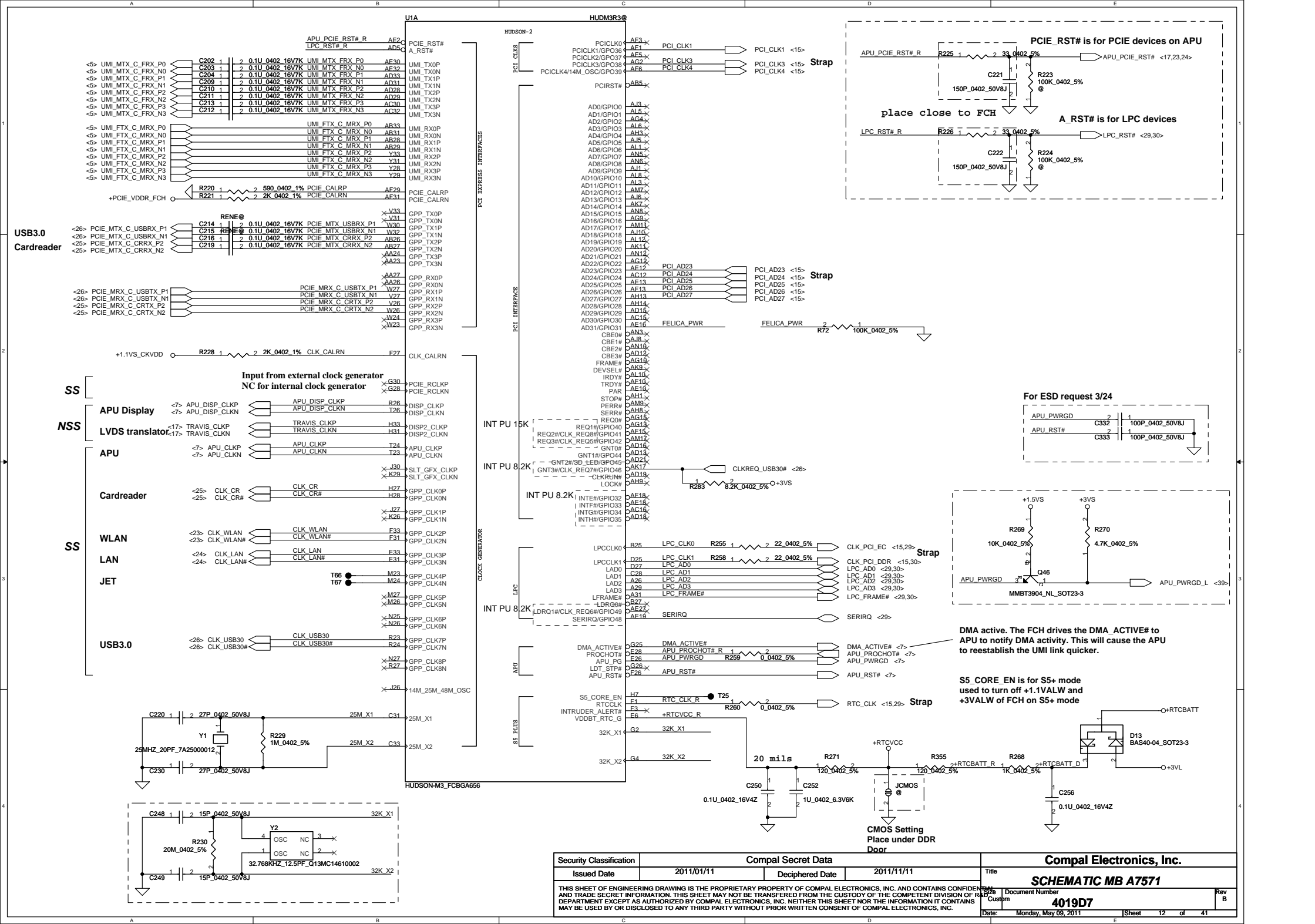
Panel PWM

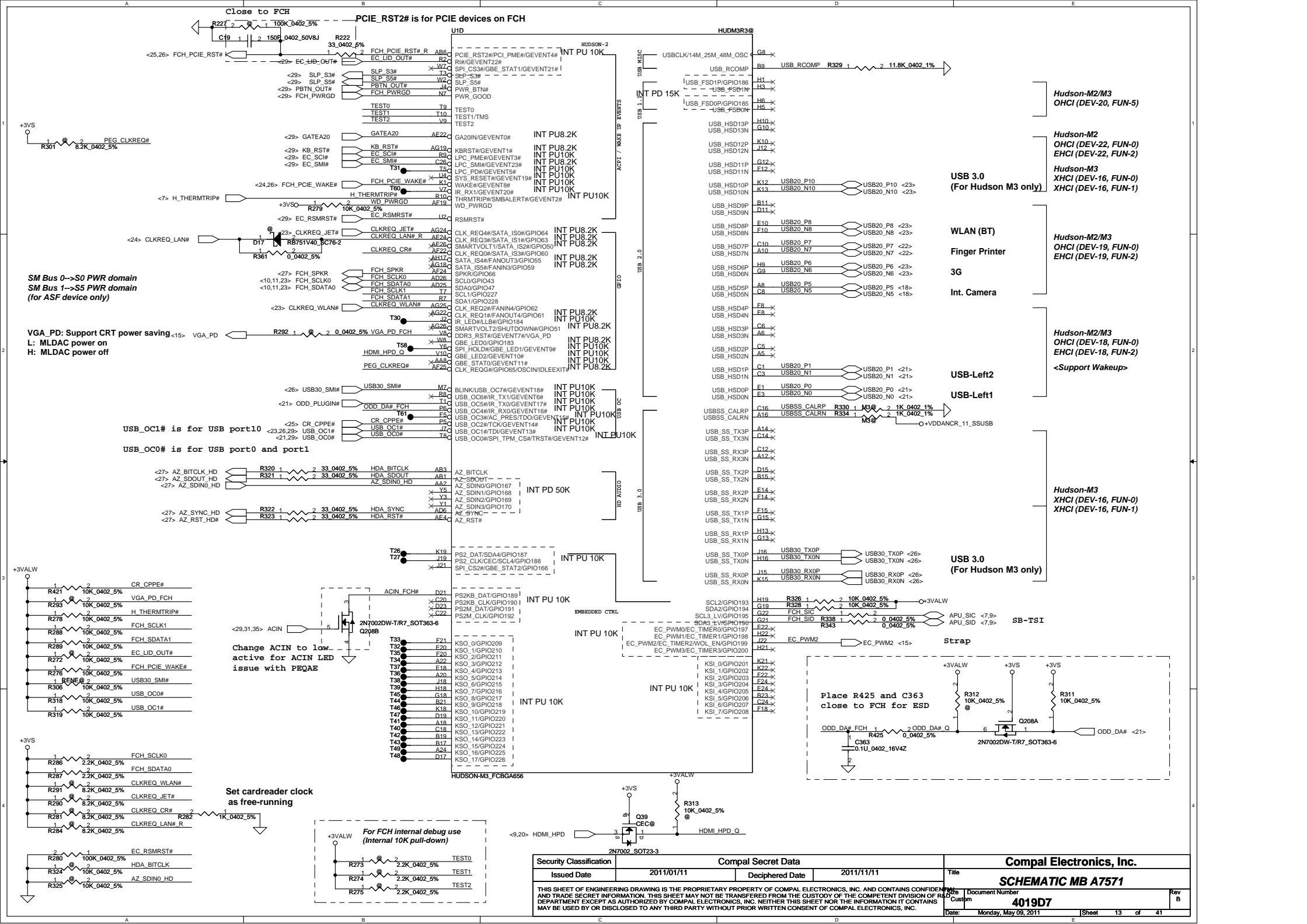


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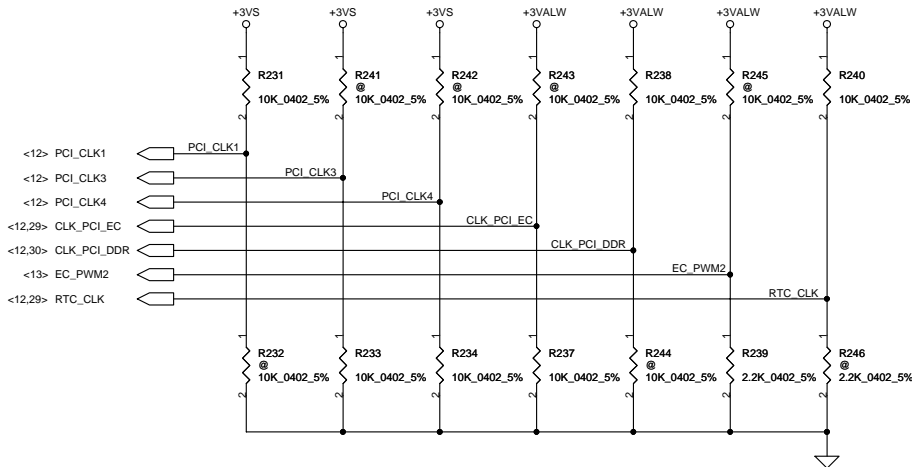
Compal Electronics, Inc.			
Title			
<i>SCHEMATIC MB A7571</i>			
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STRAP PINS

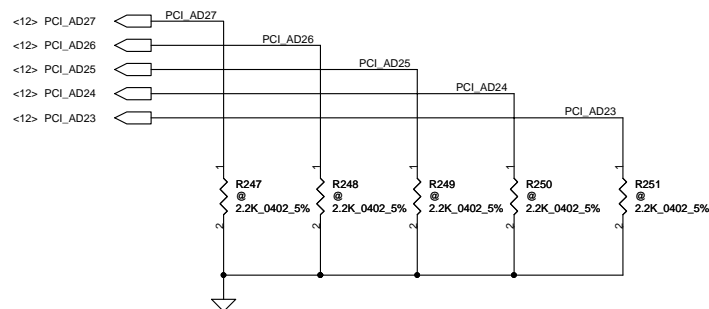
	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	ENABLE DEBUG STRAP	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM (INTERNAL 10K PULL-UP)	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	DISABLE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED



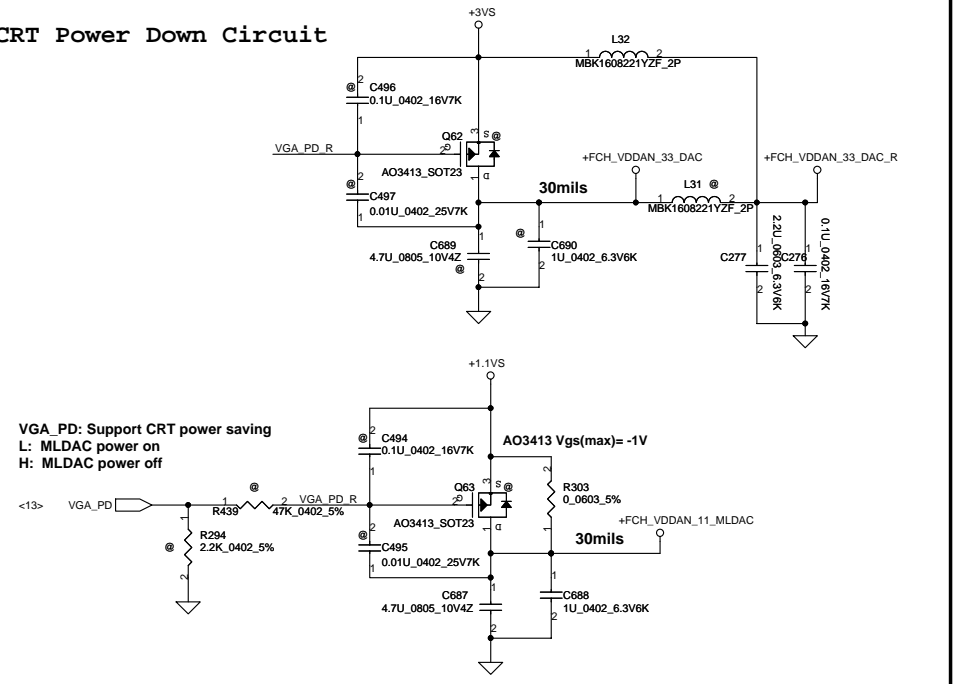
DEBUG STRAPS

FCH HAS 15K INTERNAL PU-UP FOR PCI_AD[27:23]

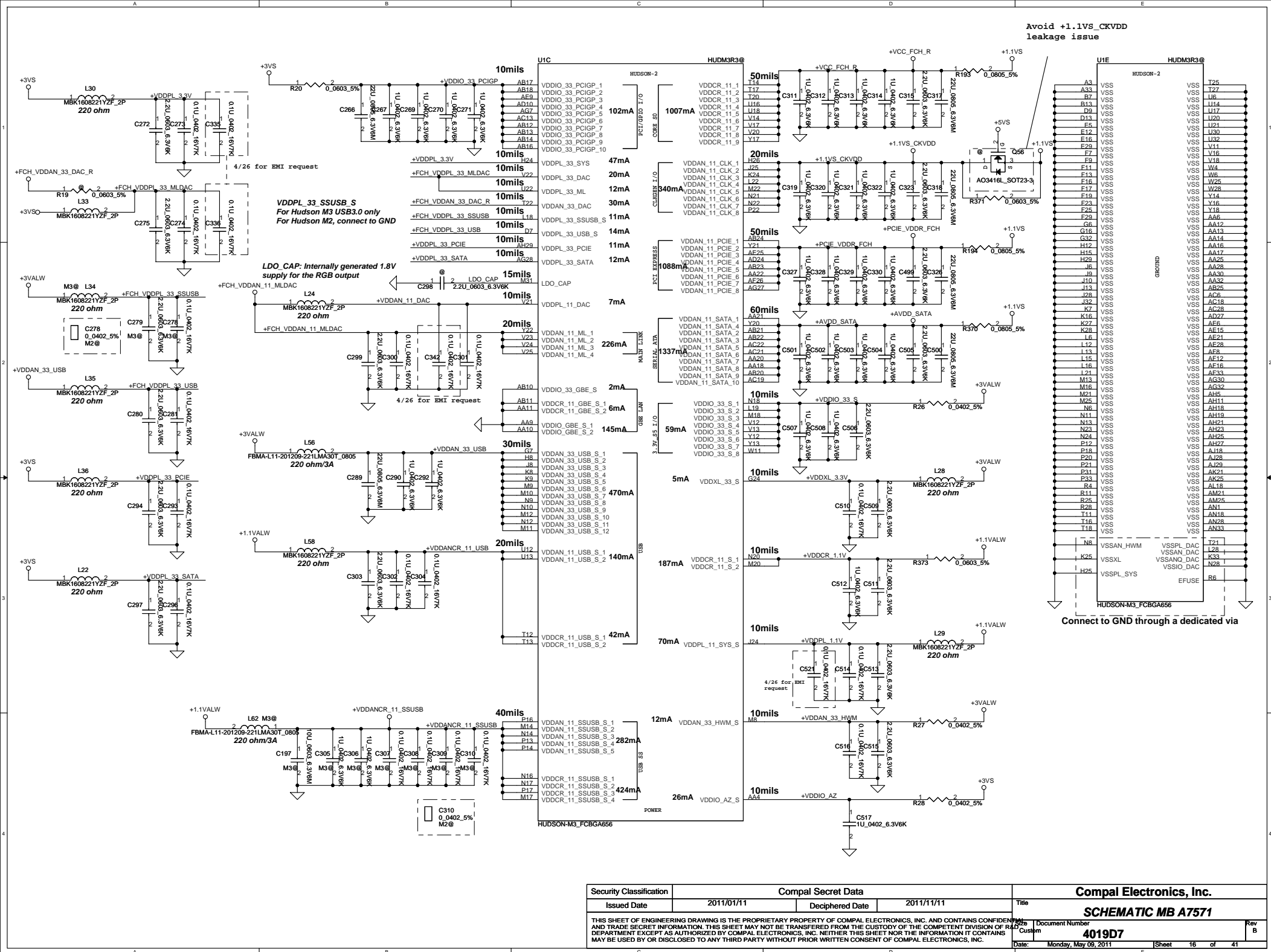
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

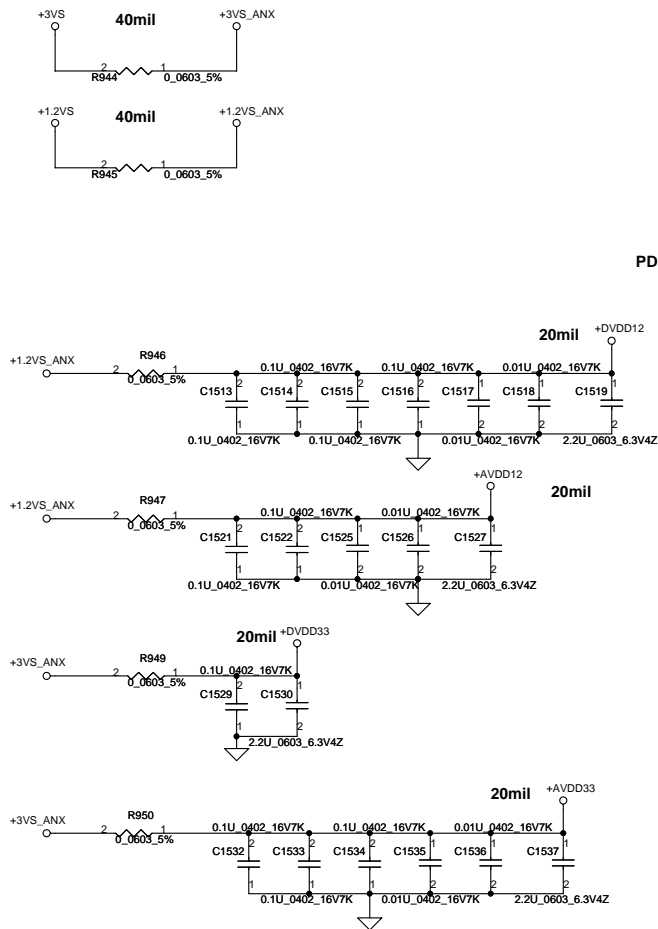


CRT Power Down Circuit



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PD 100K at Page10

<7> DP0_AUXN_C
<7> DP0_AUXP_C
<8> LVDS_HPD
<7> DP0_TXN0_C
<7> DP0_TXP0_C

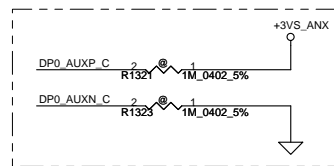
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<18> TL_ENVDD

+3VS_ANXO
R30 10K_0402_5%
C1509 0.1U_0402_16V7K

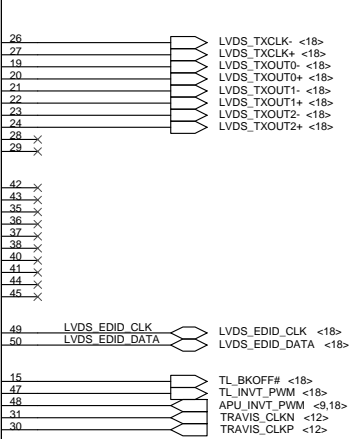
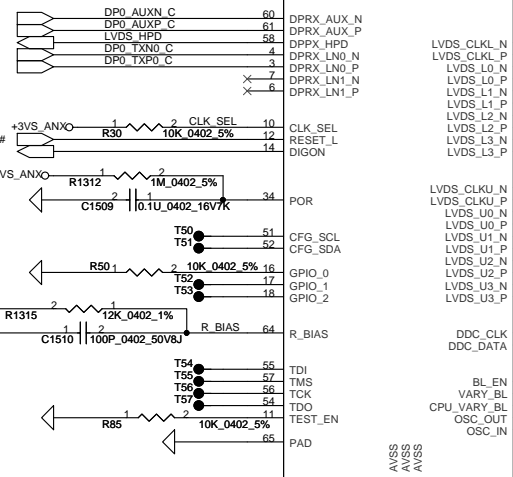
+3VS_ANXO
R1312 1M_0402_5%
C1509 0.1U_0402_16V7K

+3VS_ANXO
R1315 12K_0402_1%
C1510 100P_0402_50V8J

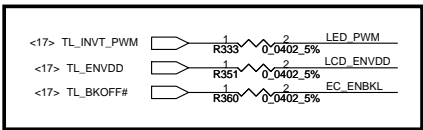
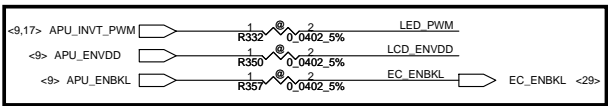
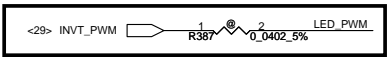
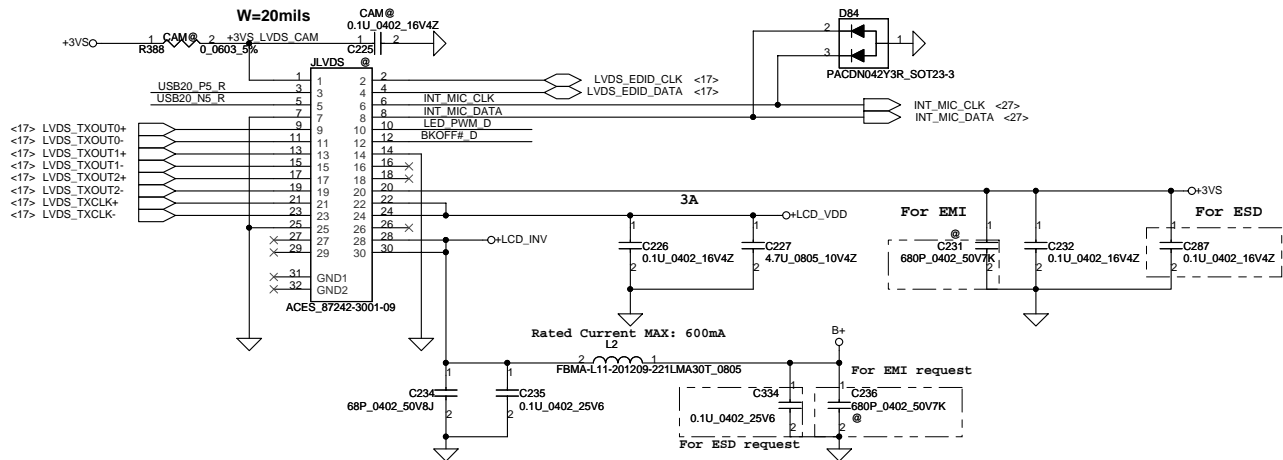
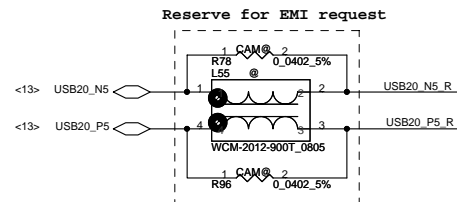
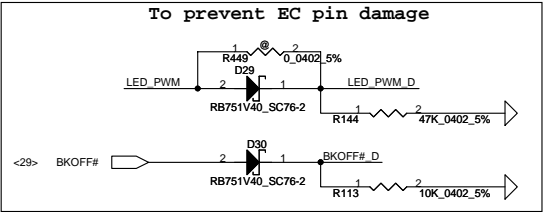
+3VS_ANXO
R85 10K_0402_5%



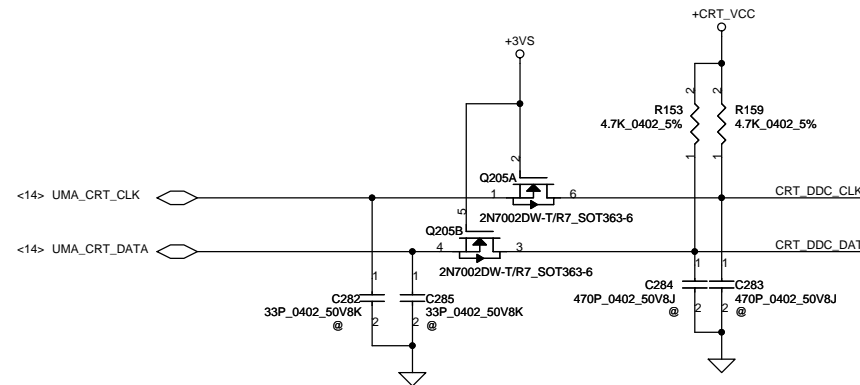
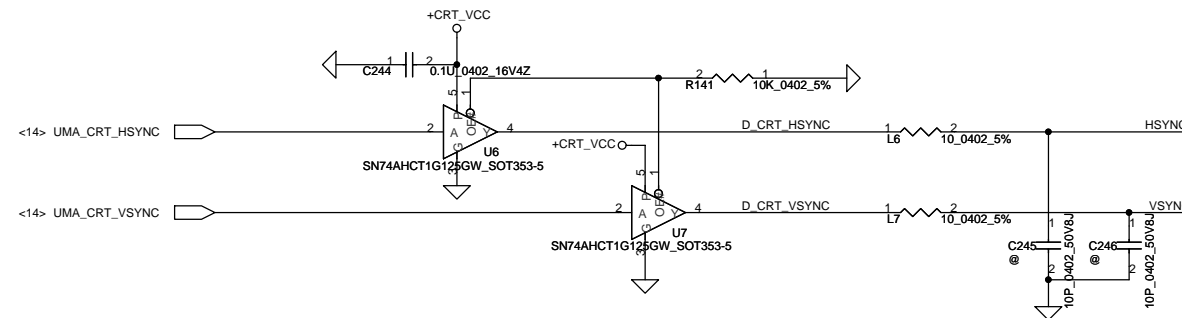
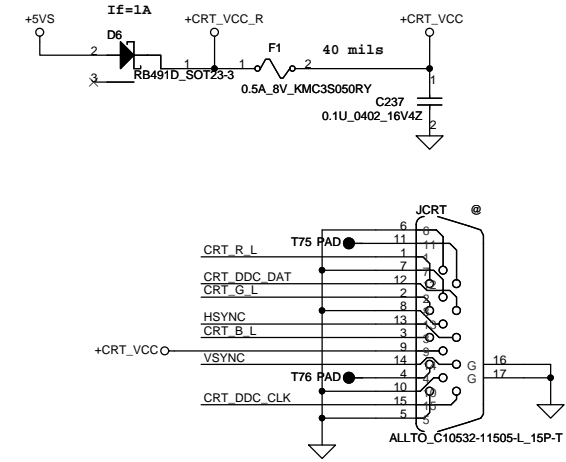
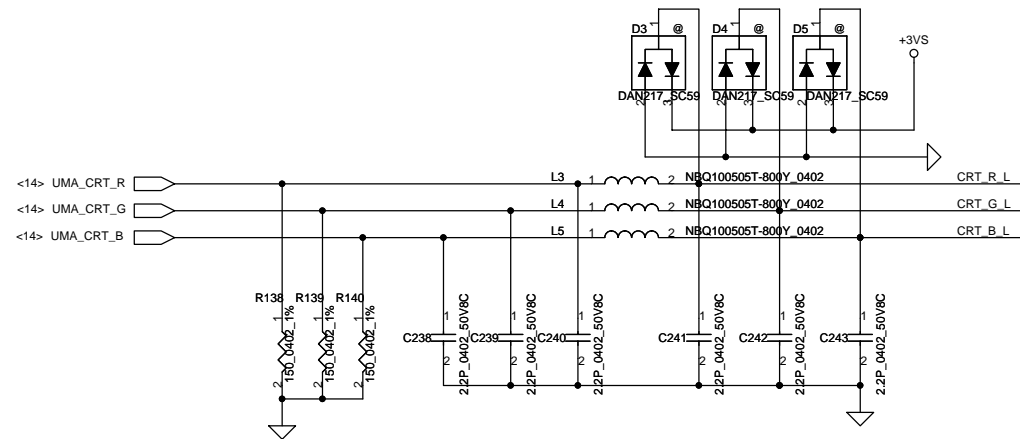
Place via on each trace bus and let resistor very close the via.



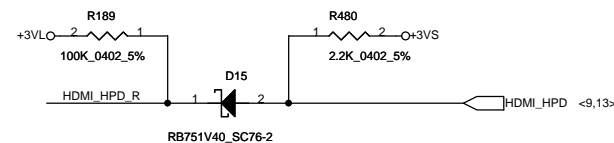
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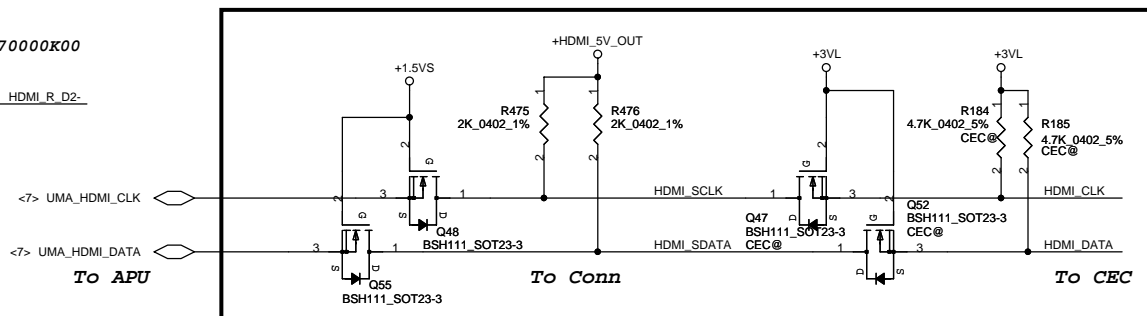
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[illegible]

JHDMI

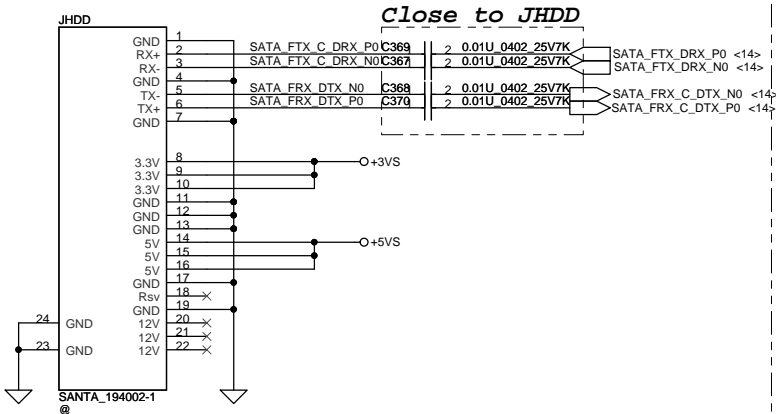
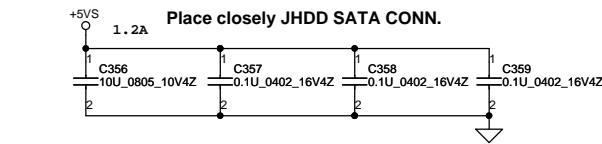
Signal	Pin
HP_DET +5V	19
DDC/CEC_GND	18
SDA	17
SCL	16
Reserved	15
CEC	14
CK-	13
CK_shield	12
D0+	11
D0_shield	10
D1+	9
D1_shield	8
D2+	7
D2_shield	6
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D2+	3
D2+	2
D2+	1

① TYCO 1939864-1 19P

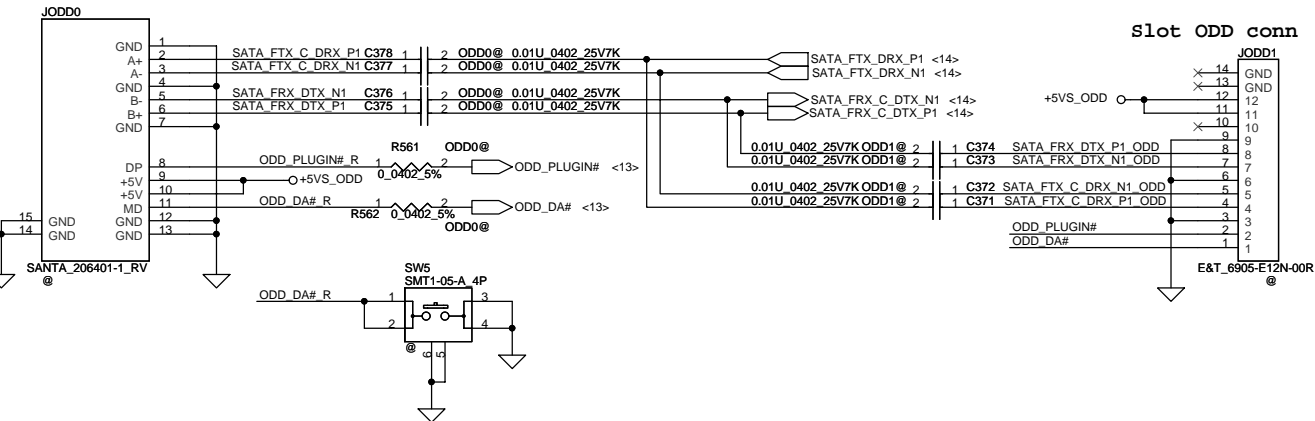
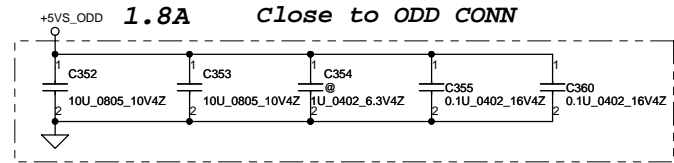


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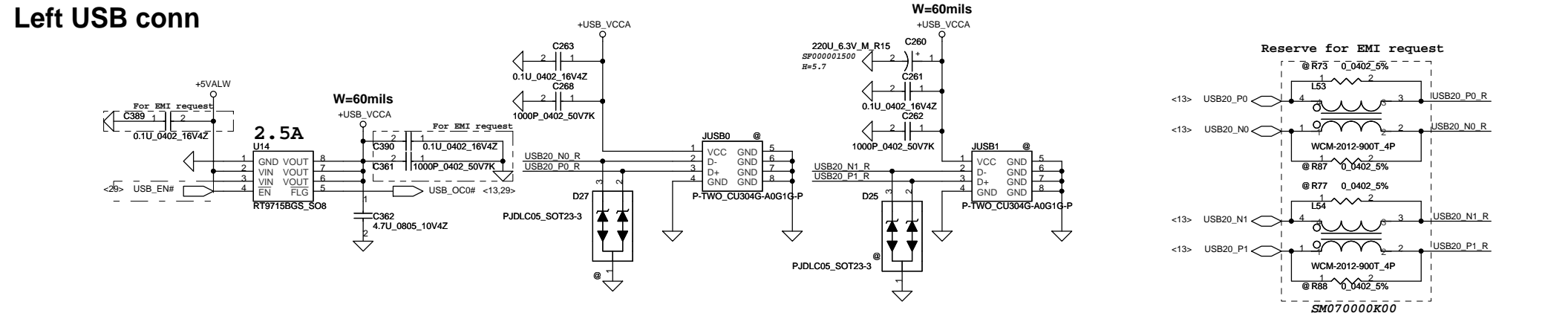
SATA HDD Conn.



SATA ODD Conn

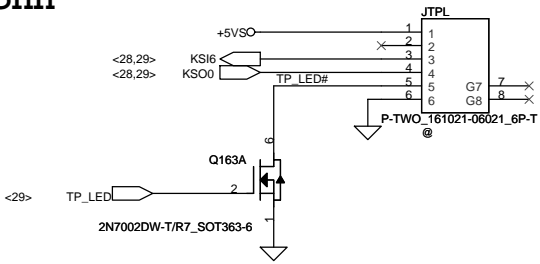


Left USB conn

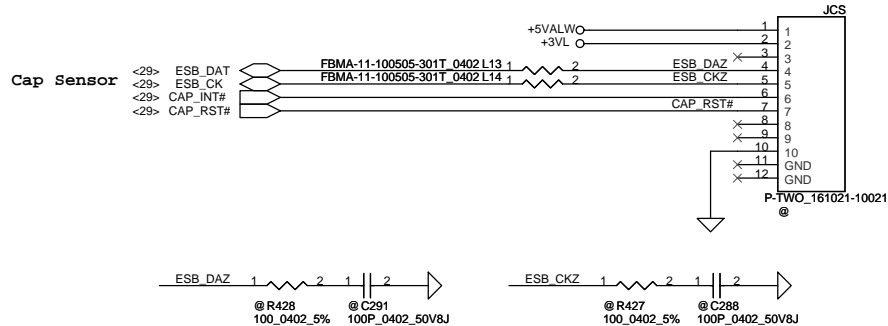


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Date: Monday, May 09, 2011		Sheet 21 of 41		Rev B	

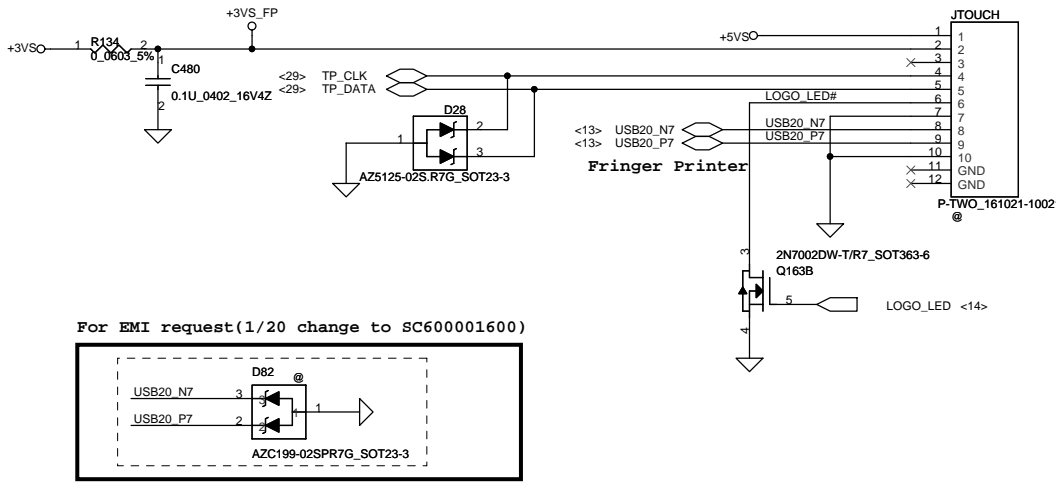
TP LED Conn



Cap Sensor Conn

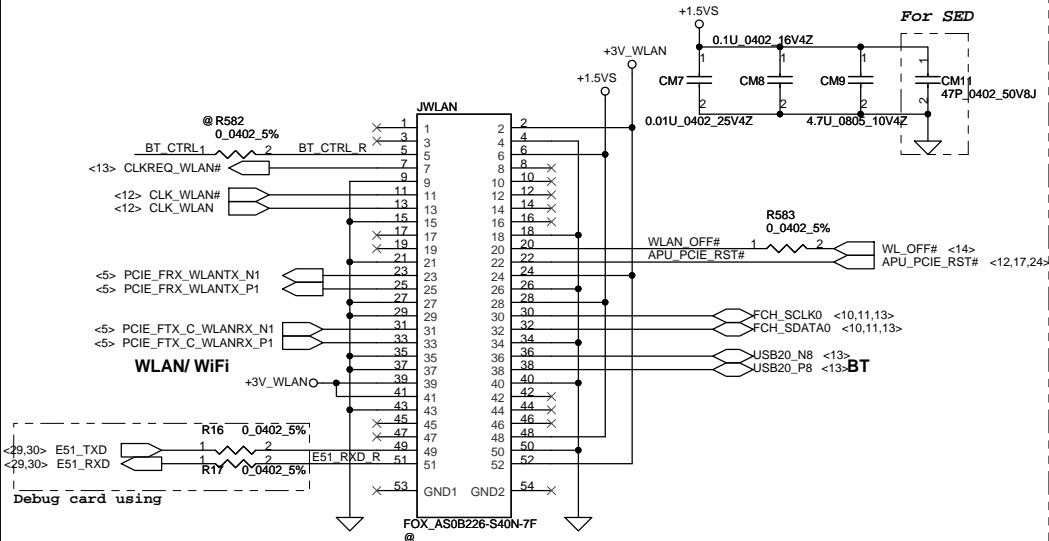
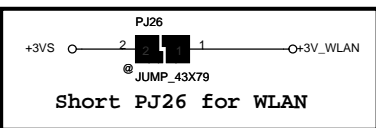


TP/B LED/B FP/B Conn

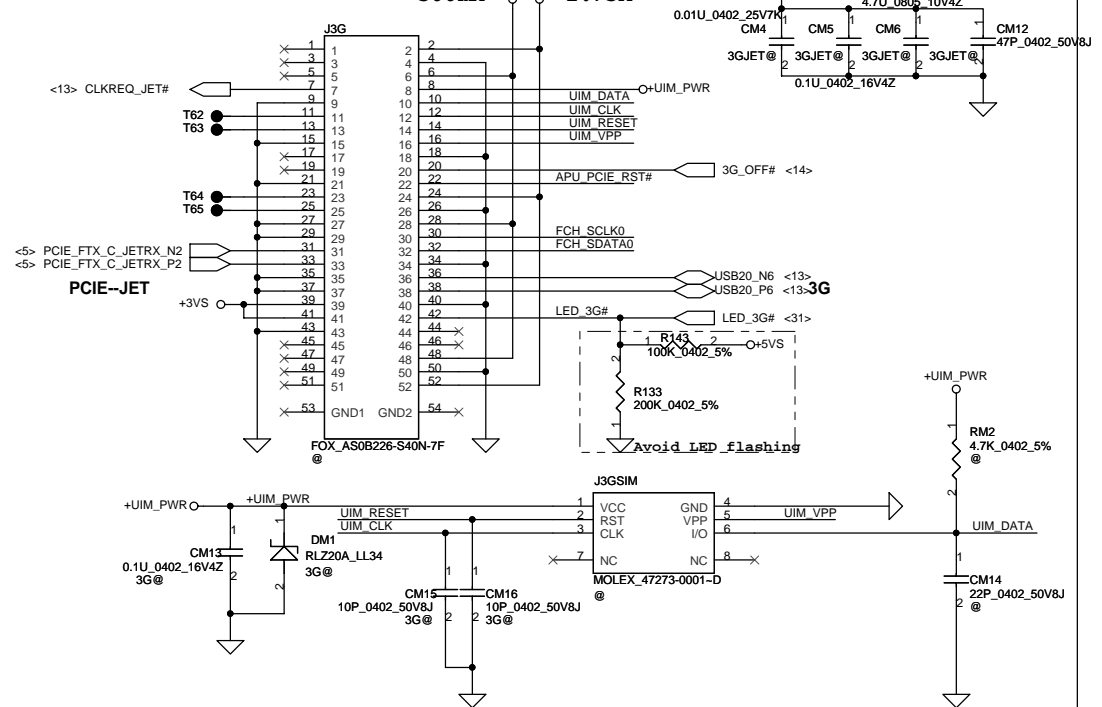


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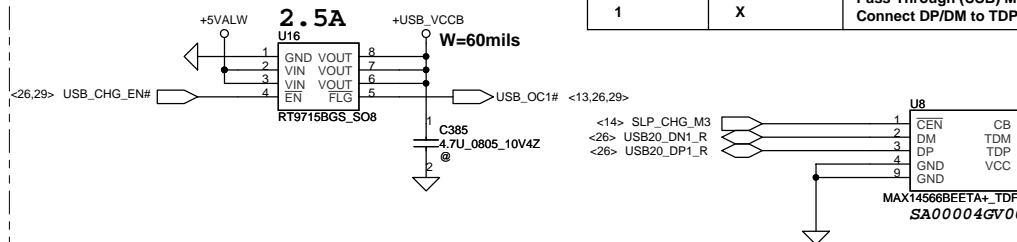
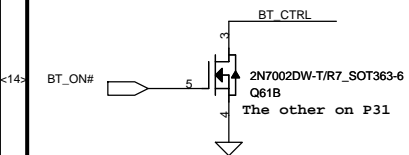
PCIe Mini Card-WLAN



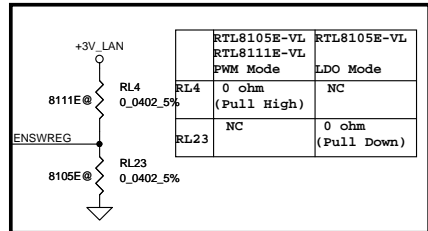
PCIe Mini Card-3G/JET



USB Sleep & Charge Auto-Mode Mode3/Mode4

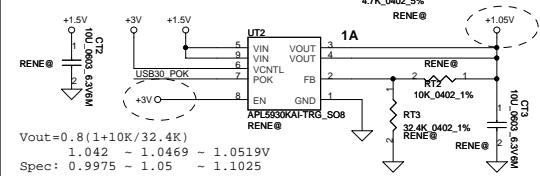


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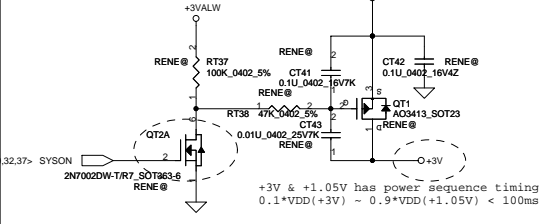


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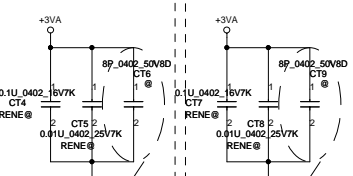
+1.5V to +1.05V Transfer



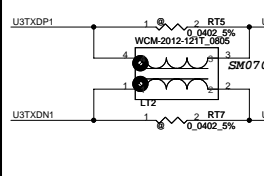
+3VALW to +3V Transfer



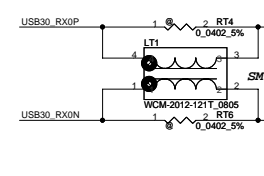
Close to U102.D7 Close to U102.P13



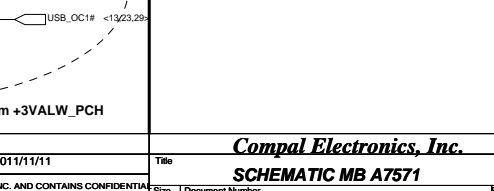
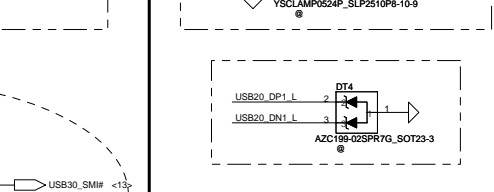
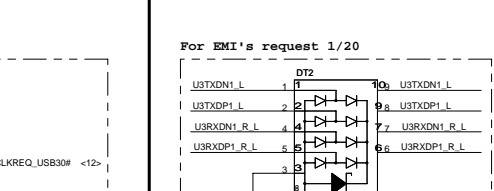
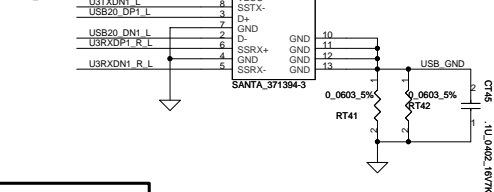
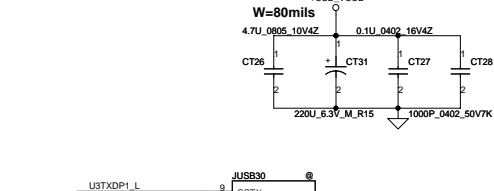
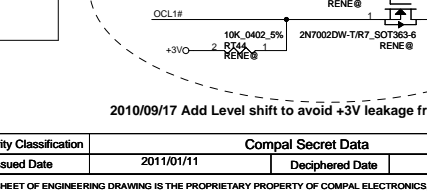
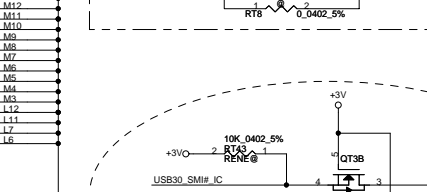
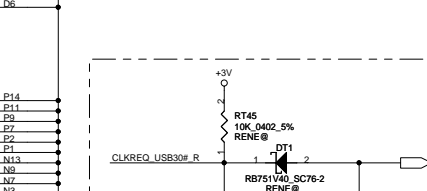
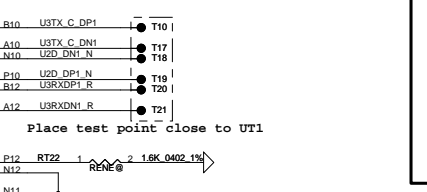
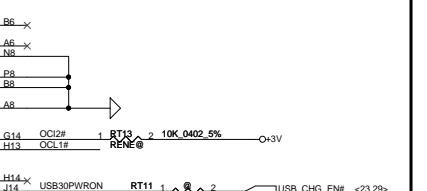
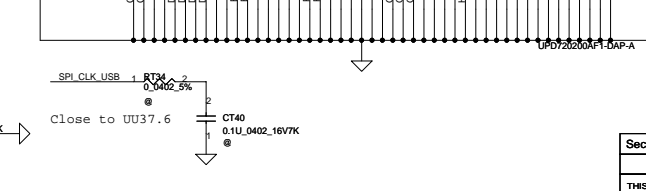
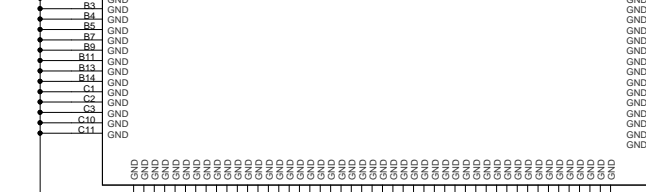
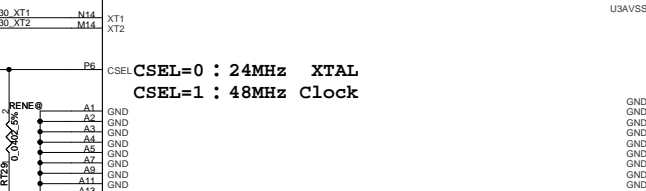
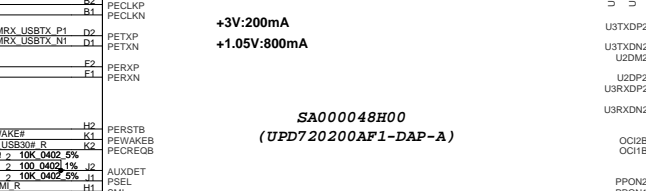
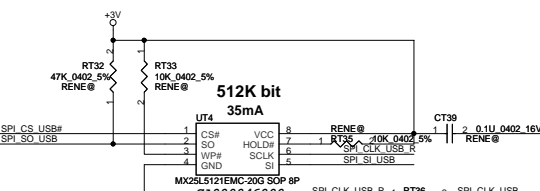
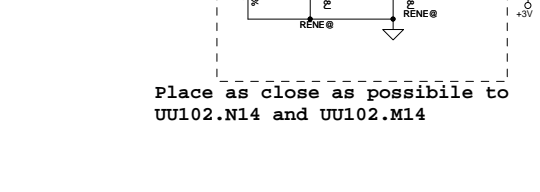
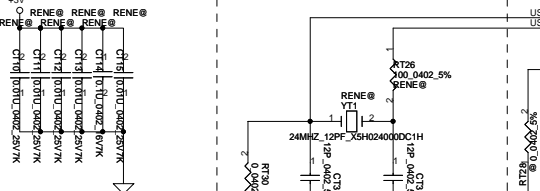
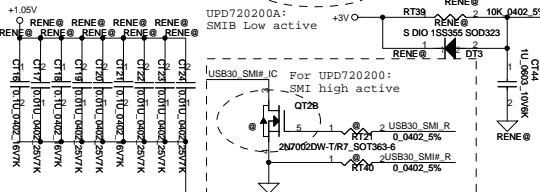
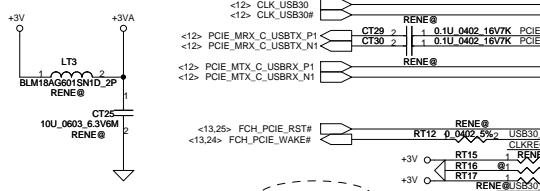
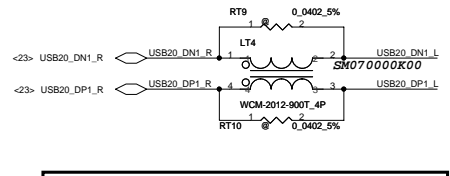
for EMI's request



for EMI's request



for EMI's request

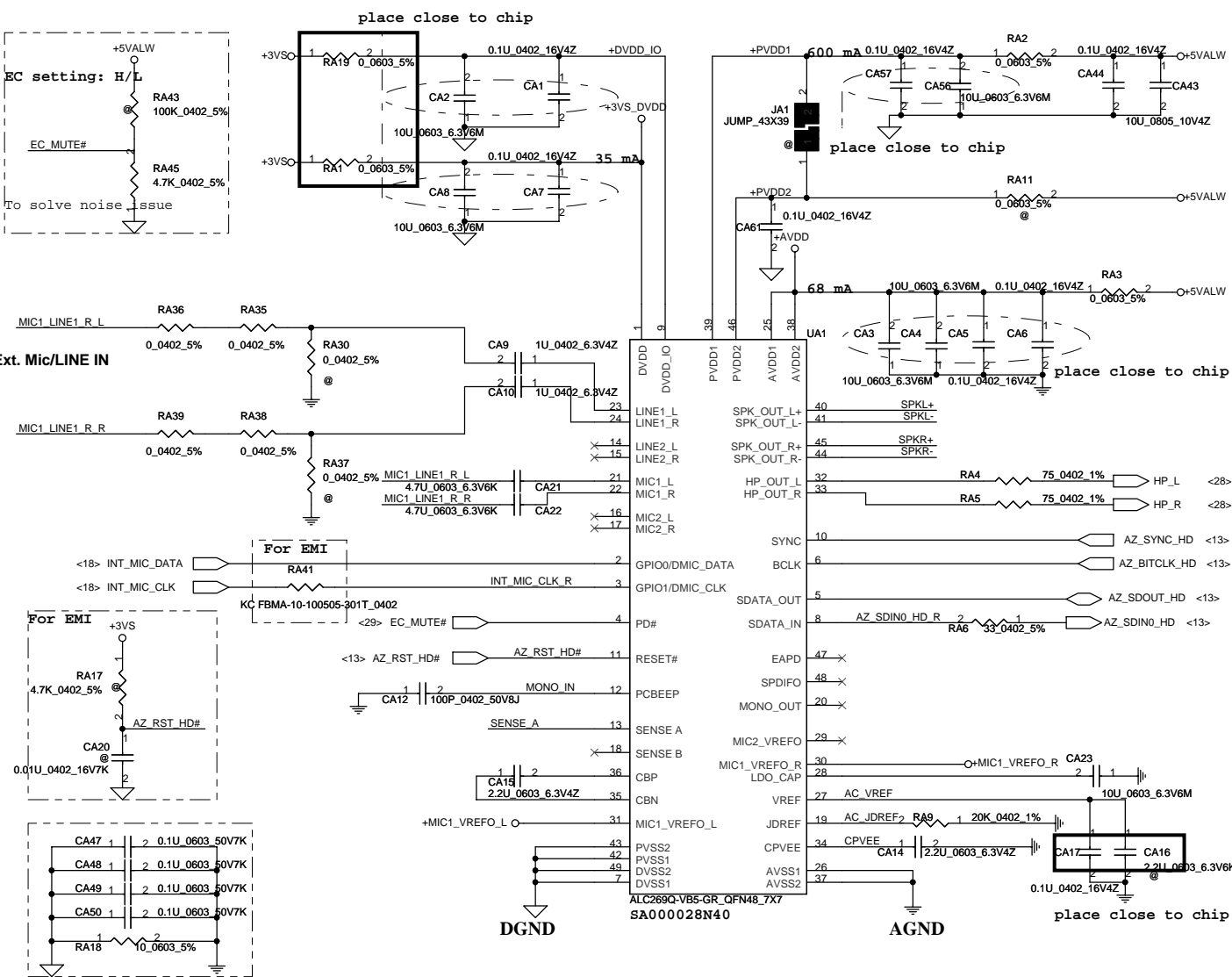


Place as close as possible to U102.N14 and U102.M14

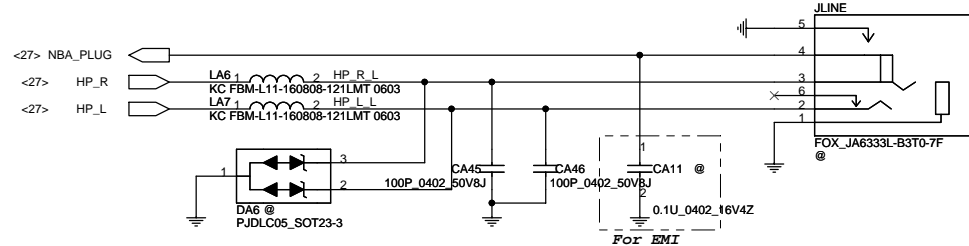
Place test point close to UT1

2010/09/17 Add Level shift to avoid +3V leakage from +3VALW_PCH

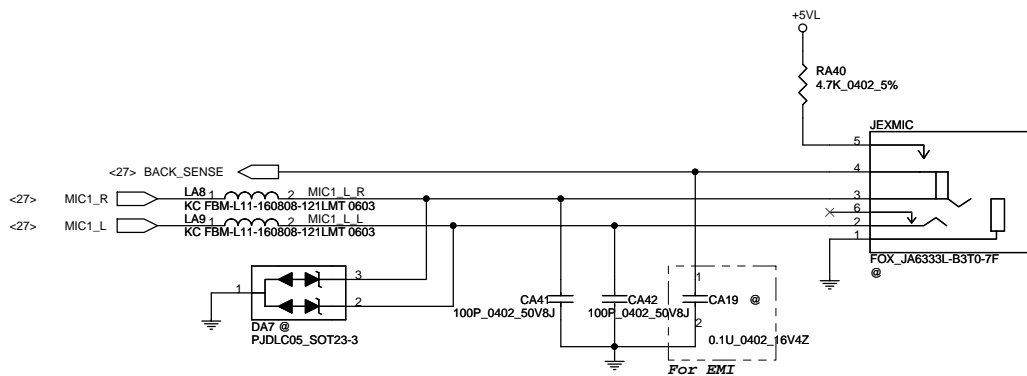
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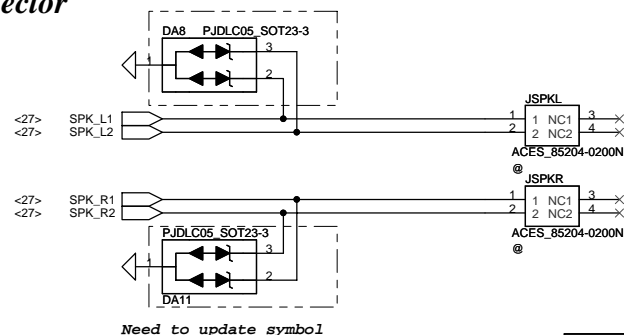
HeadPhone/LINE Out JACK



Ext.MIC/LINE IN JACK

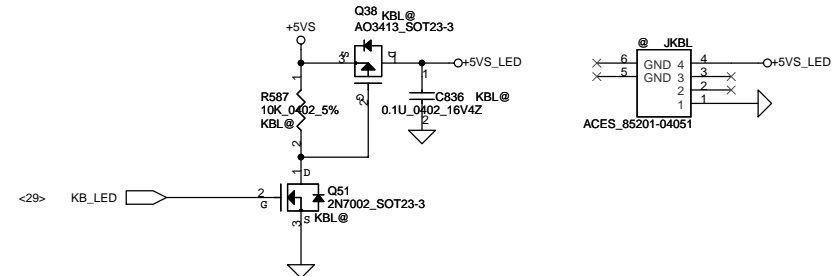


Speaker Connector



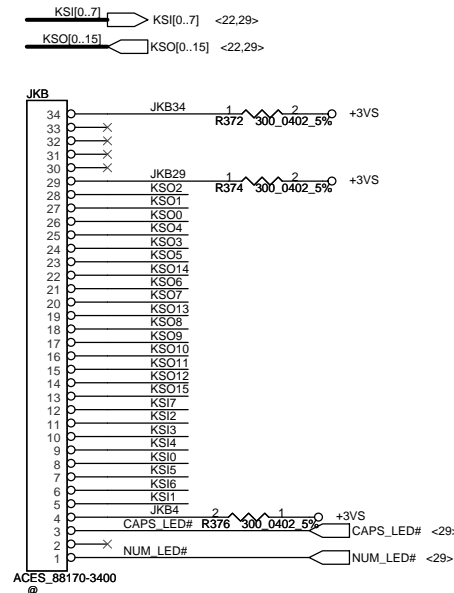
Need to update symbol

Keyboard LED



KEYBOARD CONN.

Notice: KB Connector Pin Definition Reversed with KB Membrane Pin Definition

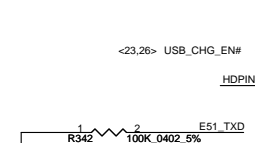
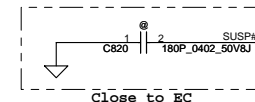
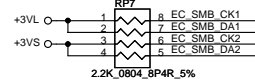
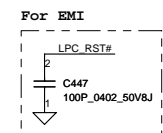
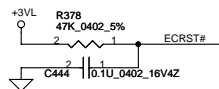
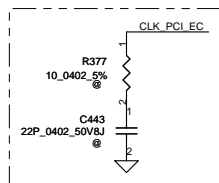


please close to JKB

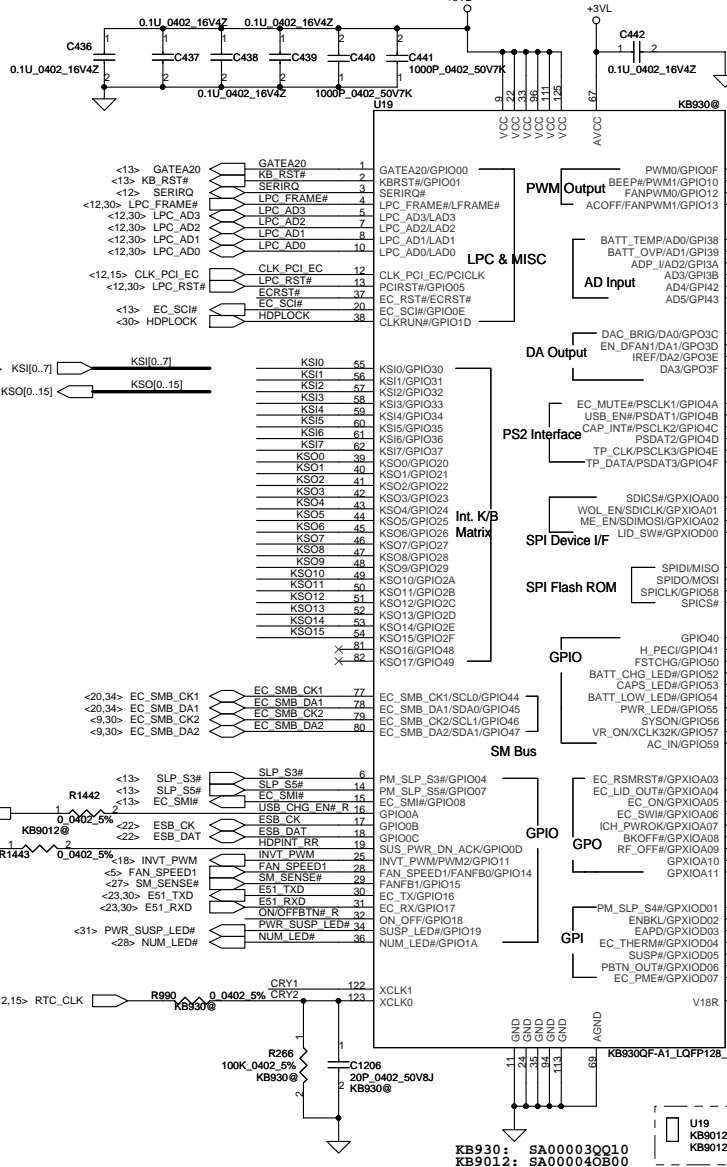
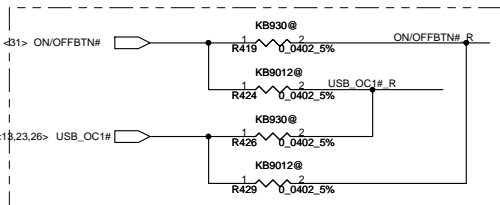
KSO2	C404	1	2	100P_0402_50V8J
KSO1	C405	1	2	100P_0402_50V8J
KSO0	C406	1	2	100P_0402_50V8J
KSO4	C407	1	2	100P_0402_50V8J
KSO3	C408	1	2	100P_0402_50V8J
KSO5	C409	1	2	100P_0402_50V8J
KSO14	C410	1	2	100P_0402_50V8J
KSO6	C411	1	2	100P_0402_50V8J
KSO7	C412	1	2	100P_0402_50V8J
KSO13	C413	1	2	100P_0402_50V8J
KSO8	C415	1	2	100P_0402_50V8J
KSO9	C416	1	2	100P_0402_50V8J
KSO10	C417	1	2	100P_0402_50V8J
KSO11	C418	1	2	100P_0402_50V8J
KSO12	C419	1	2	100P_0402_50V8J
KSO15	C420	1	2	100P_0402_50V8J
KSI7	C421	1	2	100P_0402_50V8J
KSI2	C422	1	2	100P_0402_50V8J
KSI3	C423	1	2	100P_0402_50V8J
KSI4	C424	1	2	100P_0402_50V8J
KSI0	C425	1	2	100P_0402_50V8J
KSI5	C427	1	2	100P_0402_50V8J
KSI6	C429	1	2	100P_0402_50V8J
KSI1	C431	1	2	100P_0402_50V8J
CAPS_LED#	C433	1	2	100P_0402_50V8J
NUM_LED#	C435	1	2	100P_0402_50V8J

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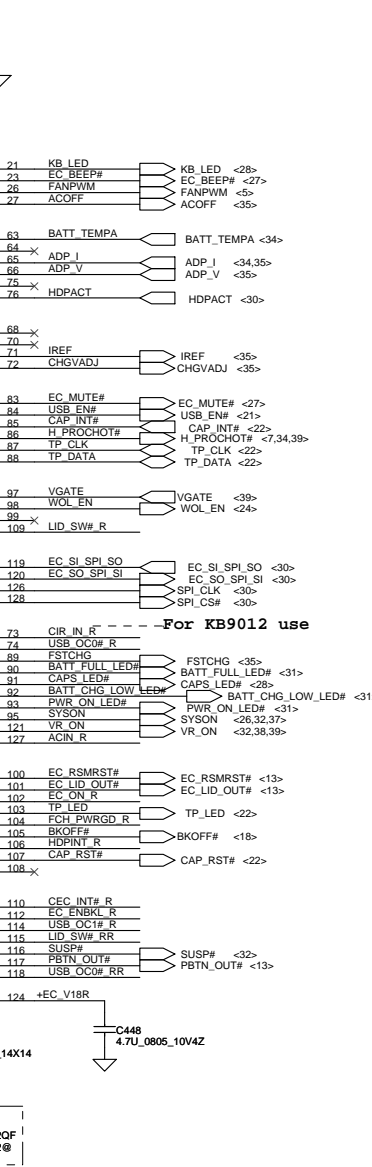
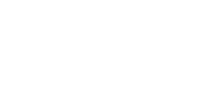
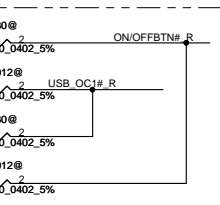
For EMI



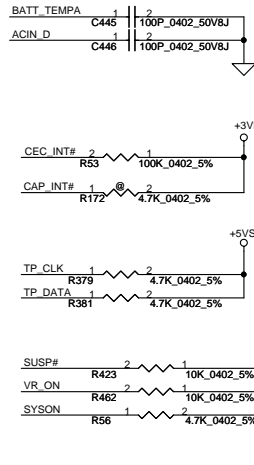
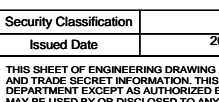
For KB930 and KB9012



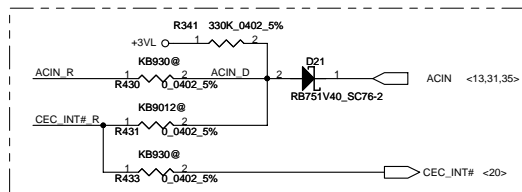
For KB930 and KB9012



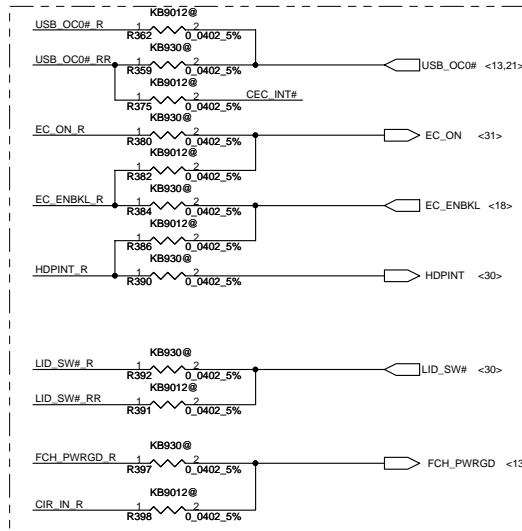
For KB930 and KB9012



For KB930 and KB9012

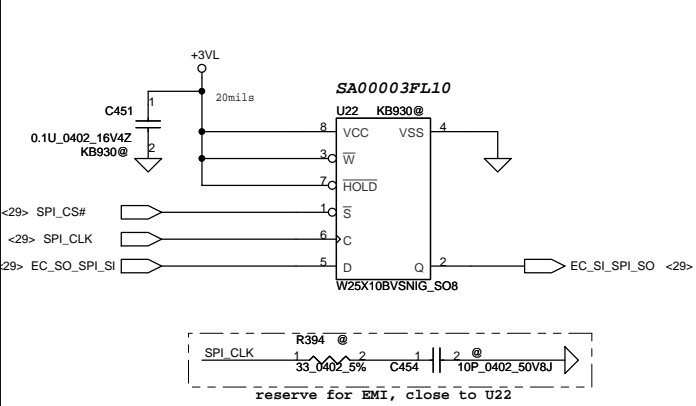


For KB930 and KB9012

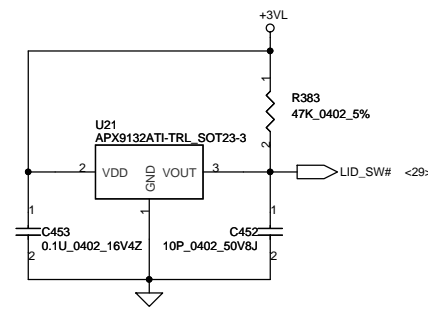


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SPI Flash (128KB)

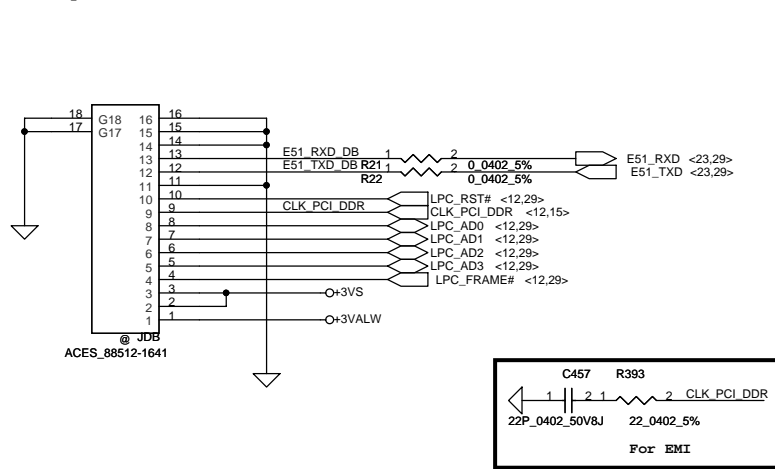


Lid SW

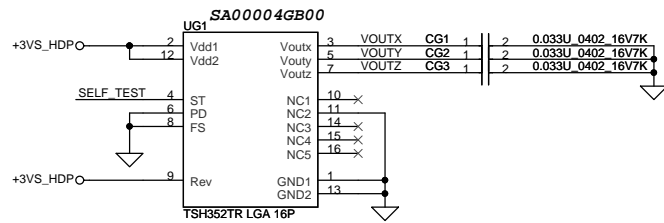
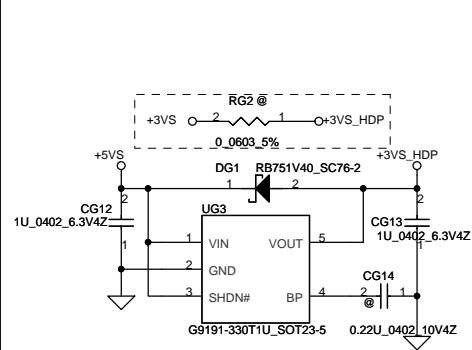


LPC / UART Debug Port

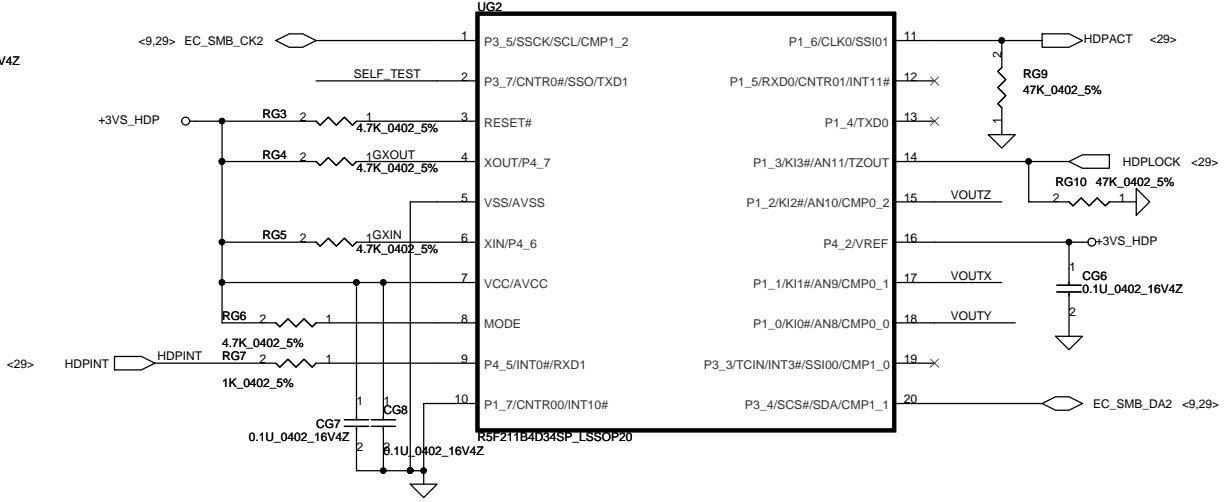
Please place JDB under DDR DIMM.



G-Sensor

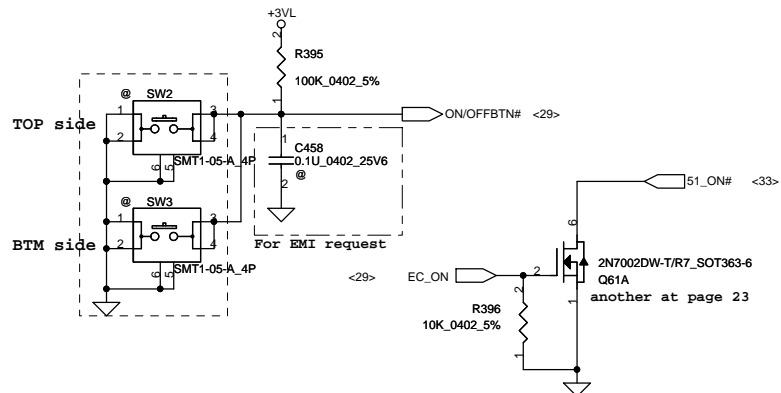


SA00003A600 Supports ODD unexpected tray eject prevention

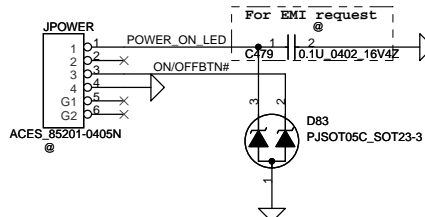


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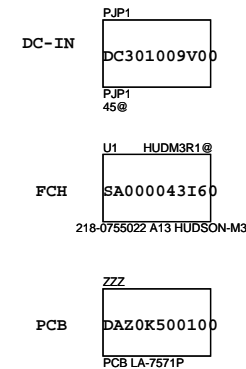
Power Button



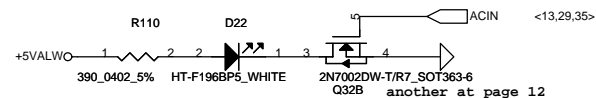
PWR/B Conn



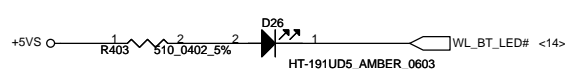
ISPD



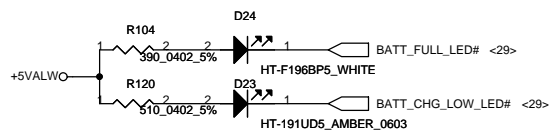
DC-IN LED



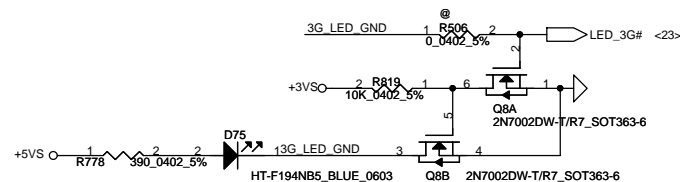
WL/BT LED



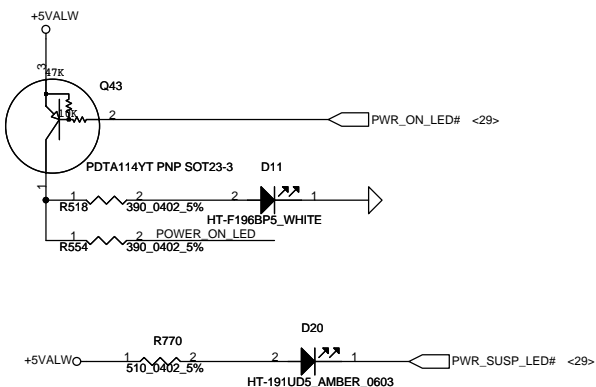
BATT CHARGE/FULL LED



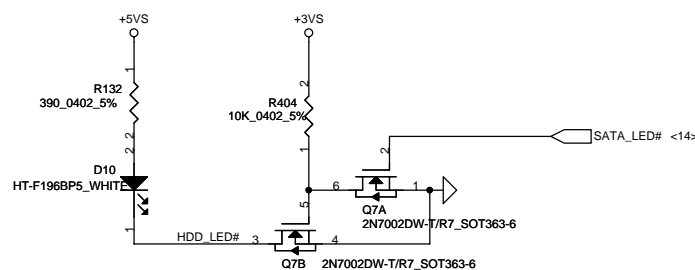
WiMAX/3G LED



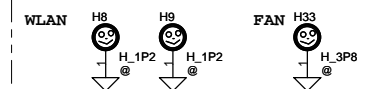
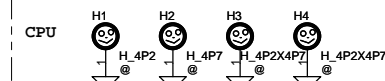
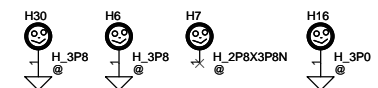
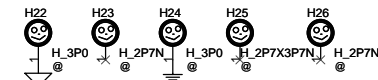
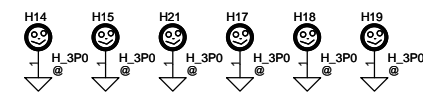
POWER/SUSPEND LED



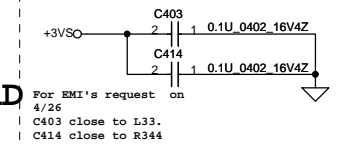
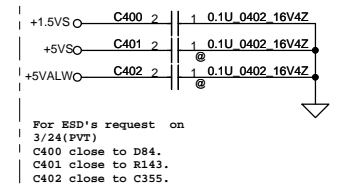
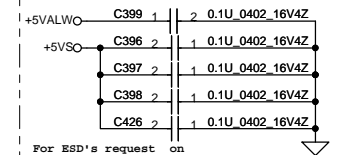
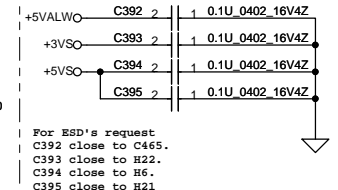
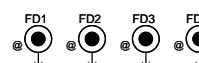
HDD LED



Screw Hole

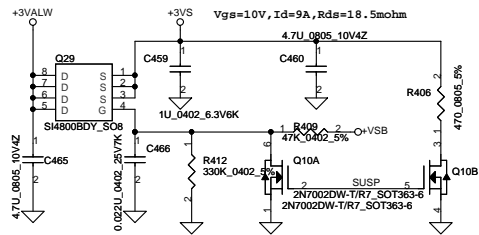


PCB Federal Mark PAD

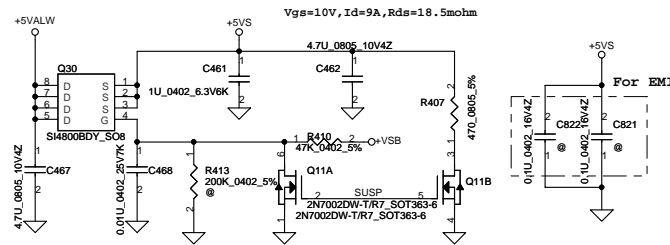


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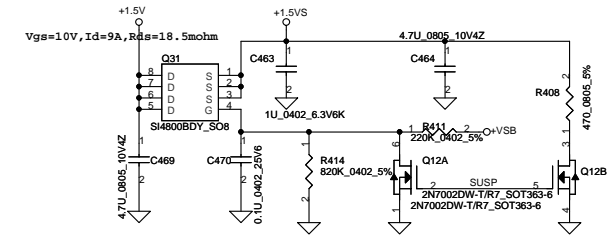
+3VALW TO +3VS



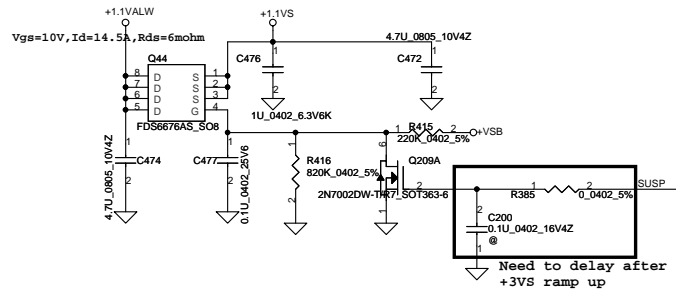
+5VALW TO +5VS



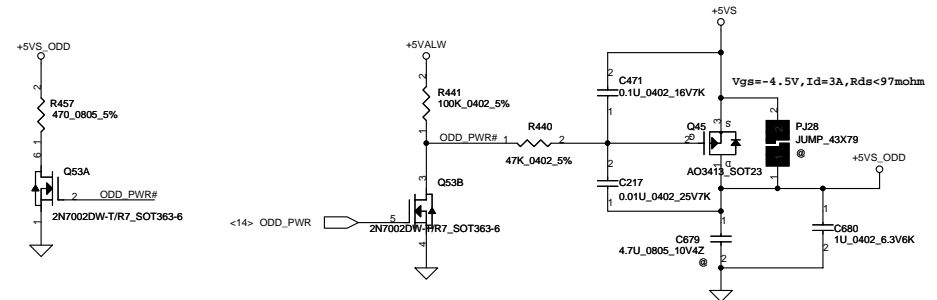
+1.5V to +1.5VS



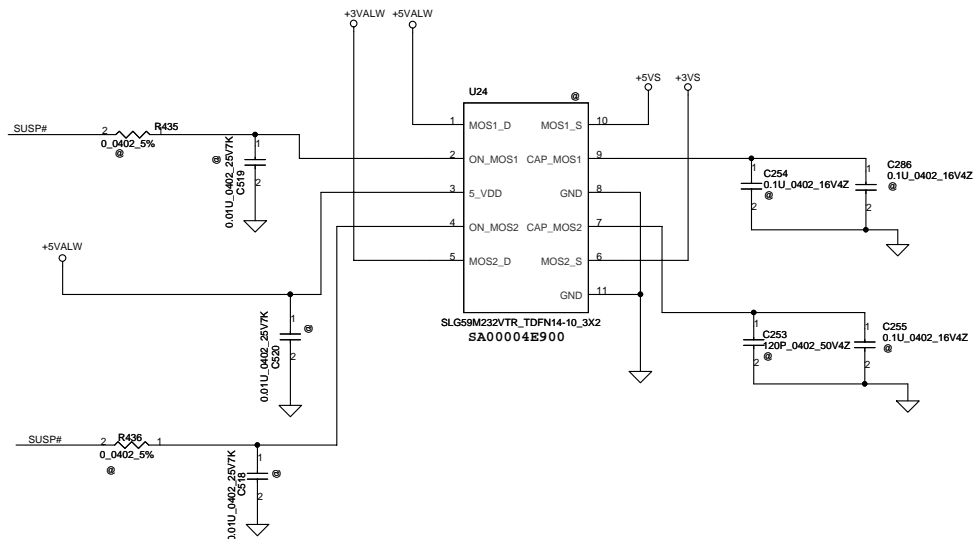
+1.1VALW to +1.1VS



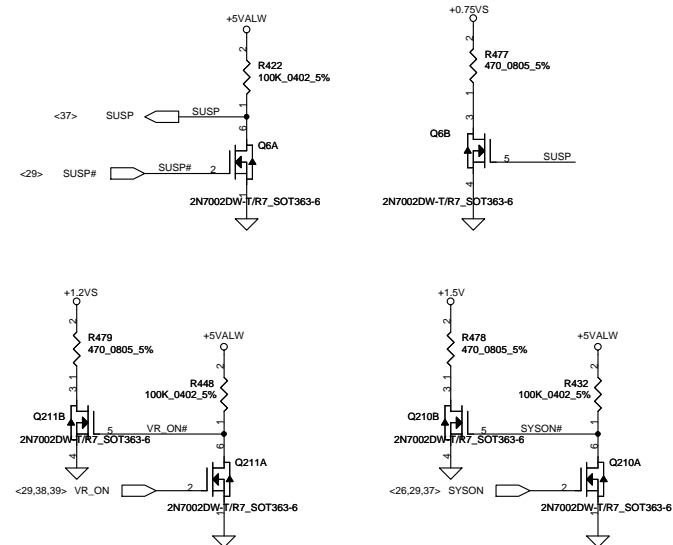
+5VS TO +5VS_ODD



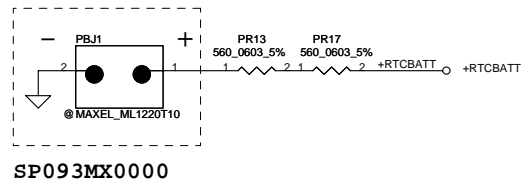
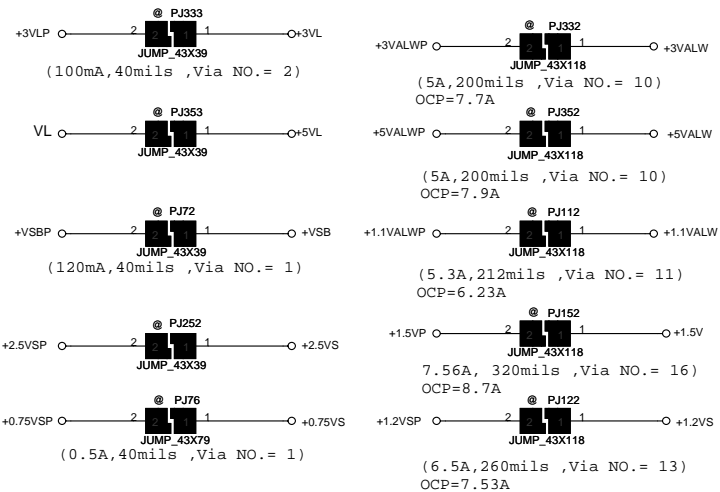
Each 250pF on CAP_MOS1 (2) will make Slew Rate(uS/V) increase of 100uS/V



Discharge

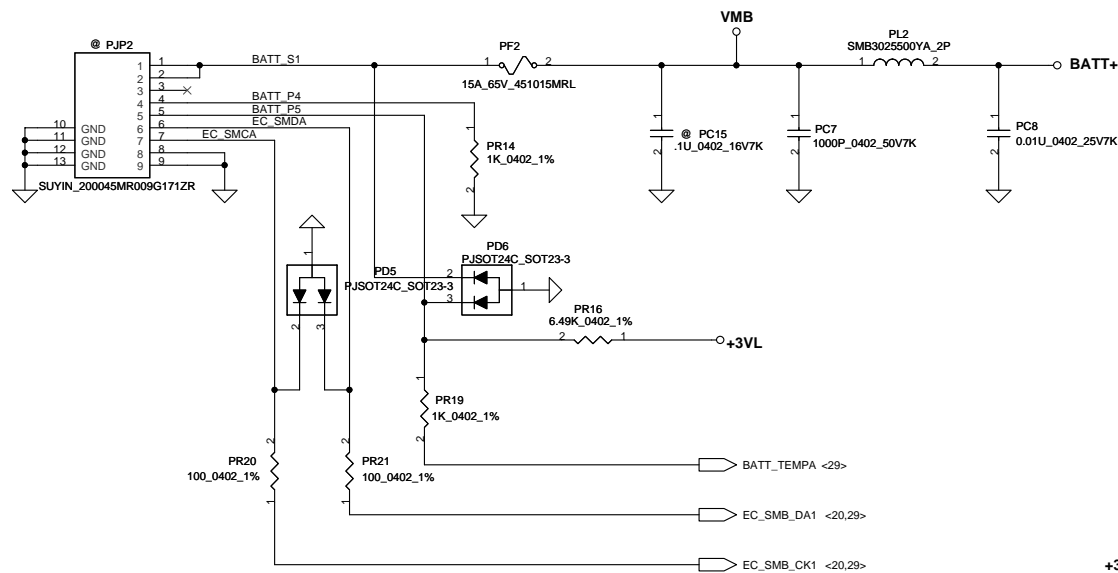


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ACIN			
	Precharge detector		
	Min.	typ.	Max
H-->L	14.42V	14.74V	15.23V
L-->H	15.39V	15.88V	16.39V

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PH1 under CPU bottom side :
 CPU thermal protection at 90 degree C
 Recovery at 56 degree C

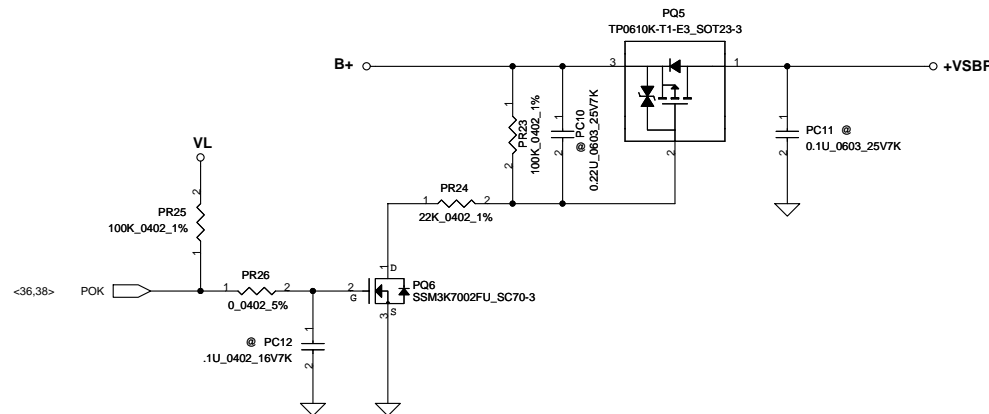
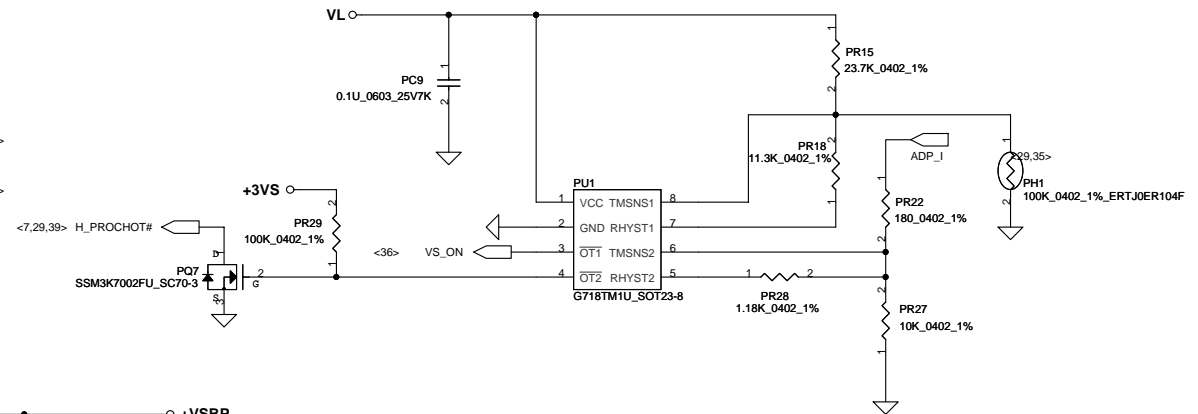
$$R_{set} = 3 * R_{tmh}$$

$$R_{hyst} = (R_{set} * R_{tml}) / (3 * R_{tml} - R_{set})$$

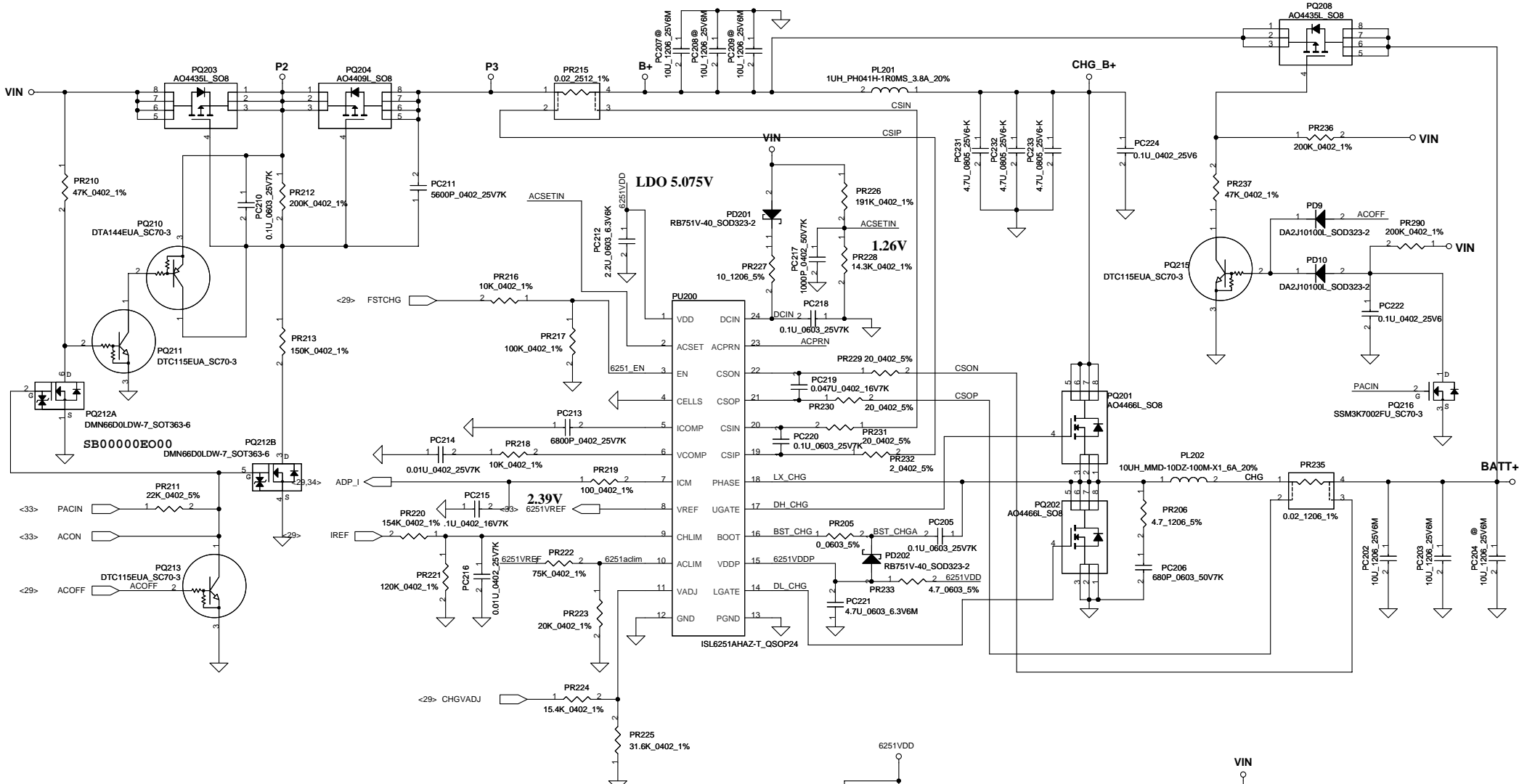
$$R_{tmh} \text{ at } 90C = 7.87K, R_{tml} \text{ at } 56C = 26.1K$$

$$R_{set} = 3 * 7.87K = 23.61K \Rightarrow 23.7K$$

$$R_{hyst} = (23.7K * 26.1K) / (3 * 26.1K - 23.7K) = 11.33K \Rightarrow 11.3K$$



Adapter	CPSETIN	Throttle Watt	Recovery Watt	Throttle Point	Recovery Point
65W_UMA	no use	71.8W	62.45W	1.504V	1.308V



CC=0.25A~3.6A
 IREF=0.9133*Icharge
 IREF=0.228V~3.288V
 VCHLIM need over 88mV

Vcell	CHGVADJ
4V	0V
4.2V	1.889V
4.35V	3.30575V

CP mode CP= 92%*Iada

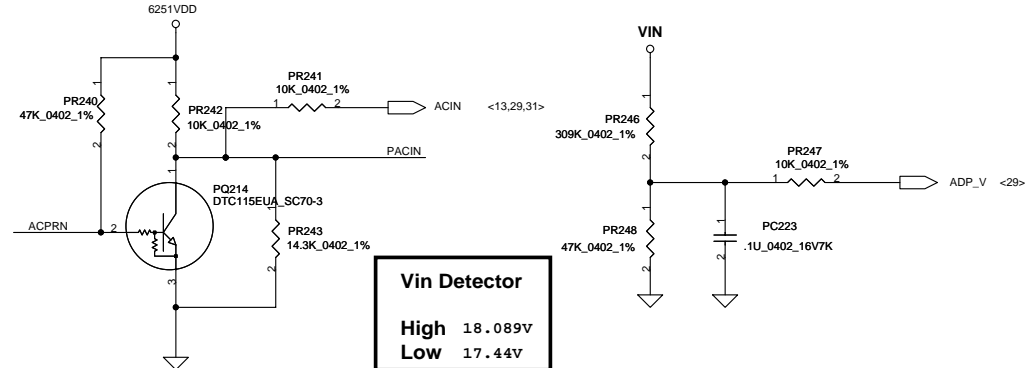
UMA

Iada=0~3.947A(75W)

CP=3.63A

Vaclim=1.1V(75W)

PR222=24k, PR223=20k, PR215=0.02

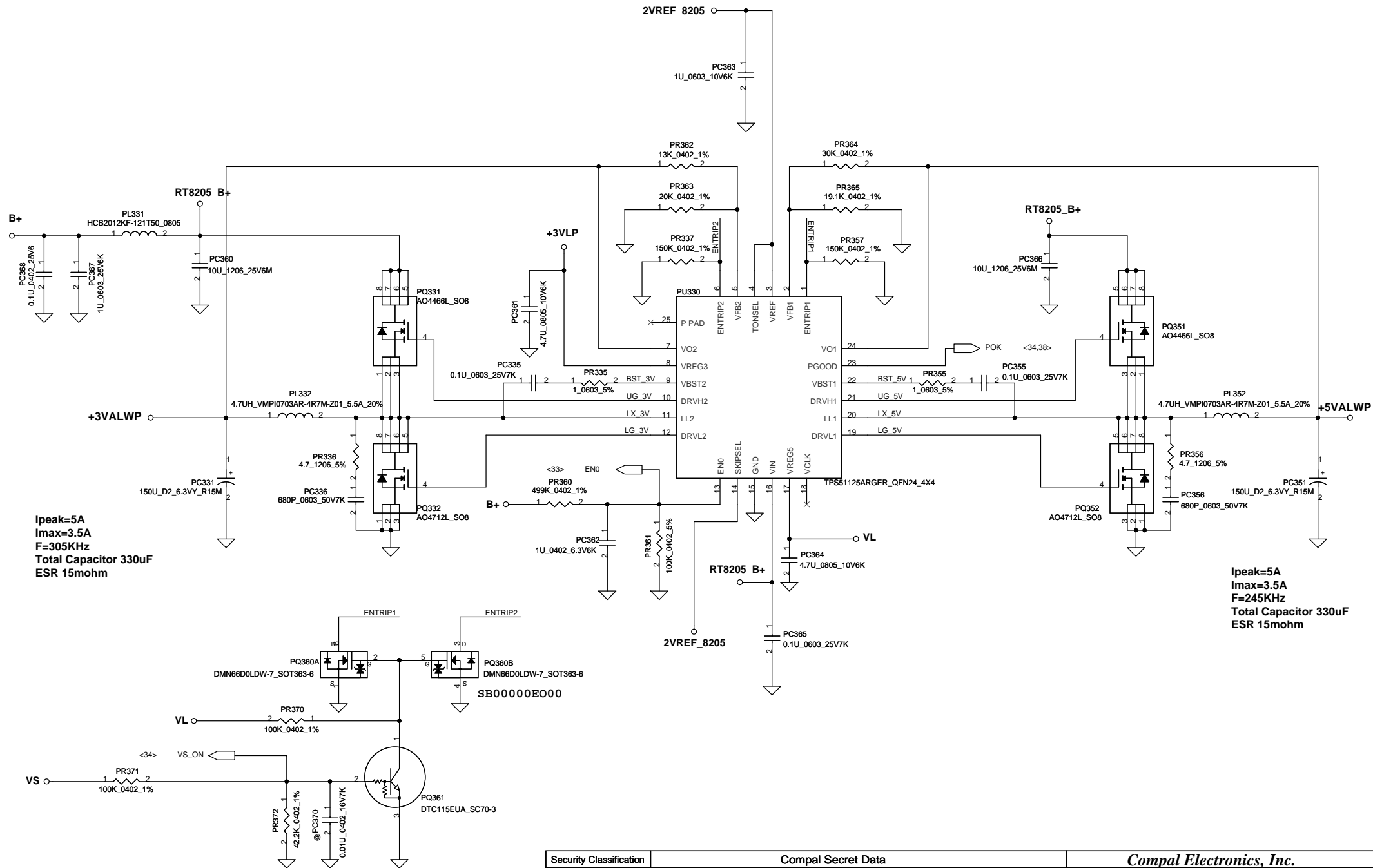


Vin Detector

High 18.089V
 Low 17.44V

$$1.26 / 14.3 * 205.3 = 18.089V$$

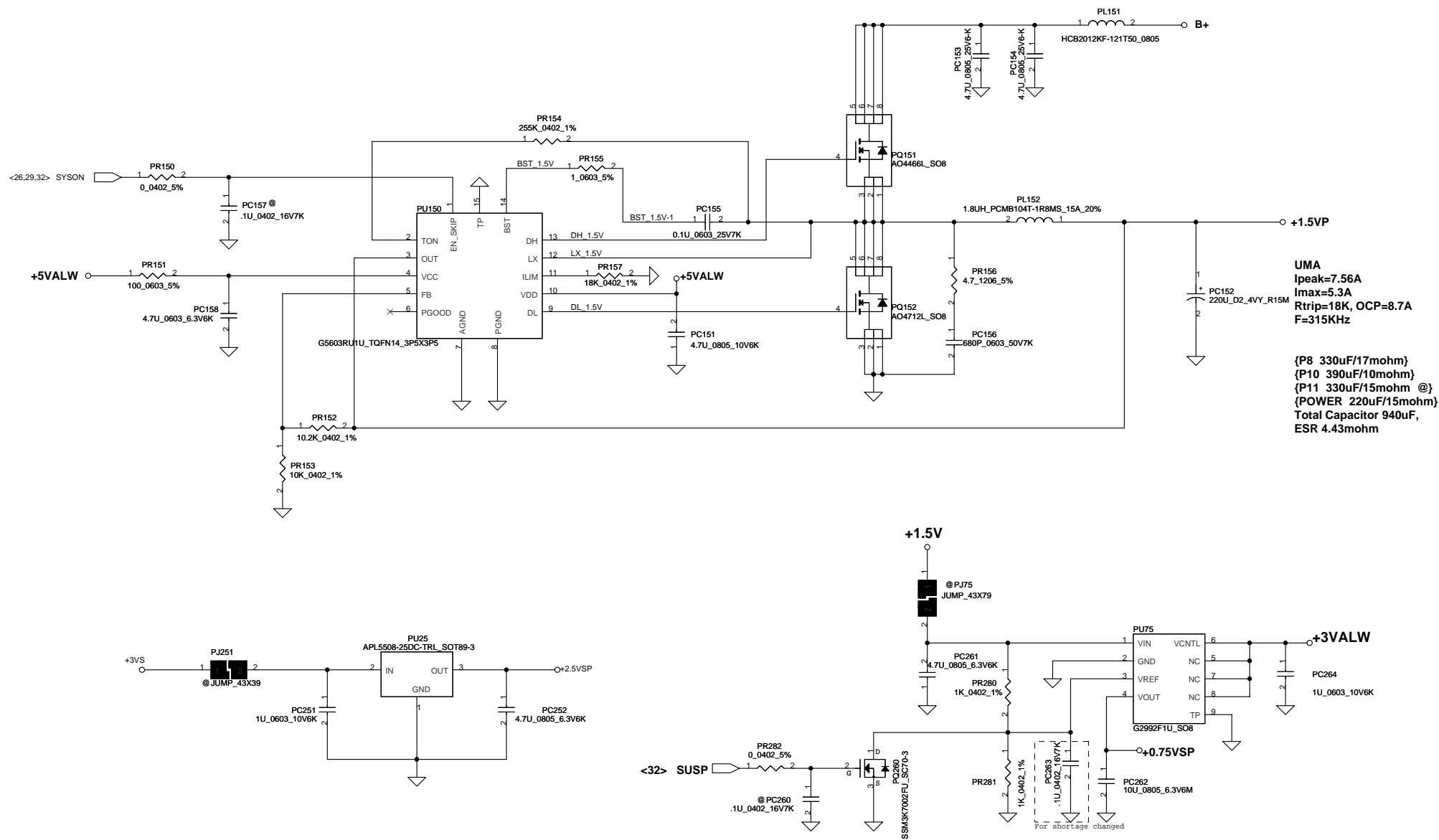
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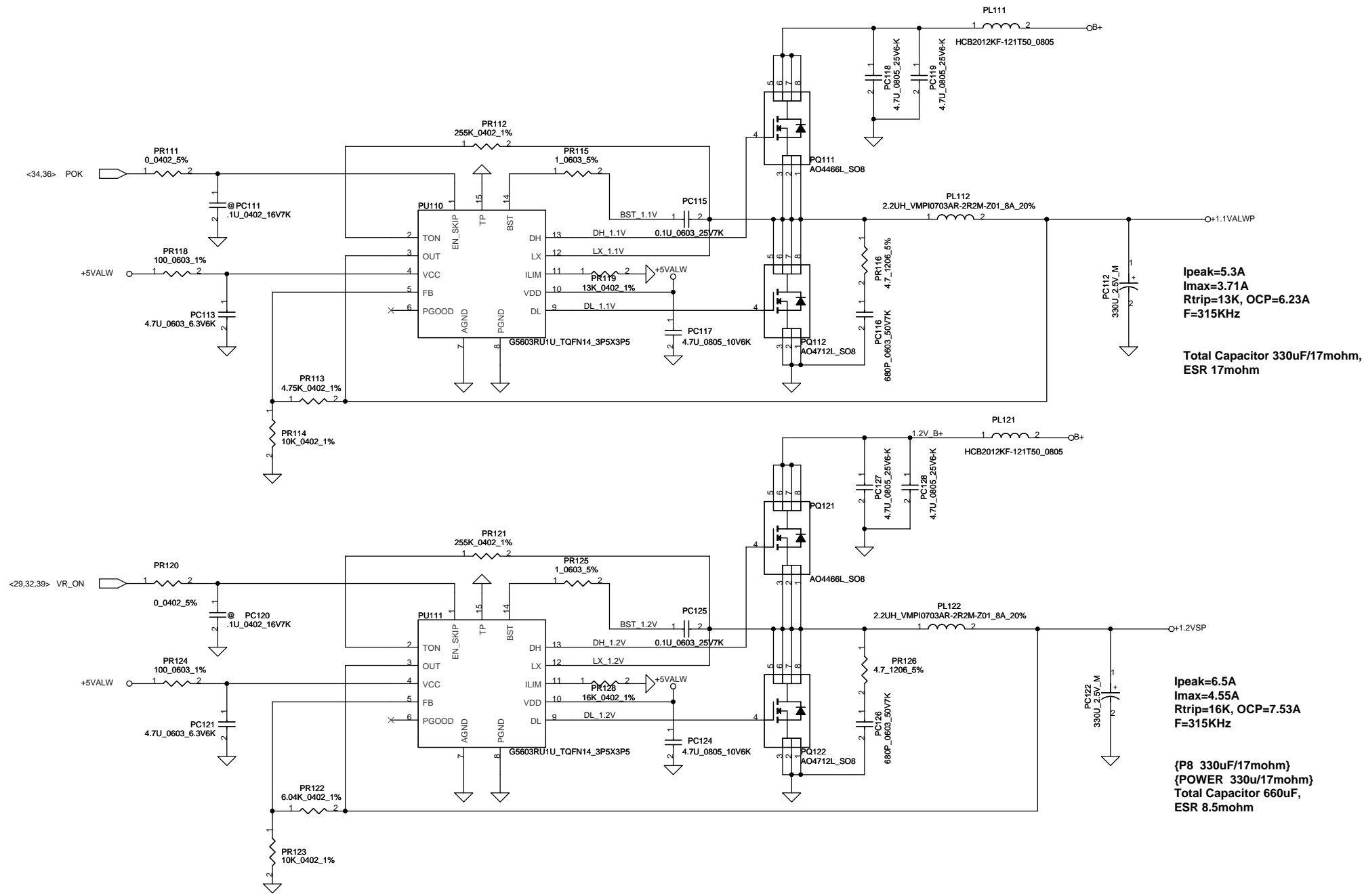
I_{peak}=5A
I_{max}=3.5A
F=305KHz
Total Capacitor 330uF
ESR 15mohm

I_{peak}=5A
I_{max}=3.5A
F=245KHz
Total Capacitor 330uF
ESR 15mohm

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2011/03/16	Page38	Change PR119/PR128 to 13K/16Kohm	For 1.1VALW/1.2VS OCP design point
2011/03/17	Page39	Change PR523 from 2.26K to 2.15Kohm	For match loadline SPEC
2011/03/21	Page37	Change PR152 from 10K to 10.2Kohm	For HW request to increase 1.5V voltage level
2011/03/21	Page35	Change PR236 & PR237 to 200K & 47Kohm	For increase BAT P-MOS divide voltage level
2011/03/21	Page34	Change PR22 & PR28 to 180 & 1.18Kohm	For 65W adapter protection point(H_PROCHOT#)
2011/03/21	Page35	Change PR222 to 75Kohm	For 65W CP protection design point
2011/03/21	Page35&36	Add PC224 & PC368 two 0.1uF/25V_0402 to GND	For EMI solution
2011/03/21	Page35~39	Add all power snuber and change boostrape R to 1ohm	For EMI solution
2011/03/21	Page35	Change PQ208 from A04407 to A04435	For 65W system
2011/03/21	Page35	Change PL202 to moding package	For short risk by QAD 8KG test

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REVISION C { 椰 特 離 躑 E: 0.2 TO 0.3

NO	DATE	PA { 缺矜 \ \ 量颯纒確淳葦掙特触葦颯鵠 \ }	PURPOSE
1.	03/15	26 Add DT4	For ESD's request
2.	03/15	13 Delete ODD_PLU { 缺確鵠耳焄焄掙那 level shift sásc@NDDkhPD	ODD has internal 1K PD
3.	03/15	25 Add level shift for CR_CPPE# leakage issue	For leakage issue
4.	03/15	13 Change { 檣纒量葦焄那PD to { 缺矜 矜箇触蜎鼻耳 \ }	{ 缺矜 矜箇触蜎耳 \
5.	03/15	24 Change LO { 缺颯焄燐矜纒 \ 丑櫟 \ 躡PI0176 and WLJBTZYED to { 缺蕪	For LED flash issue
6.	03/17	25 Change RC16 from 22 ohm to 0 ohm for SDXC performance issue	For SDXC performance issue
7.	03/17	12 Change JCOMS to JC MOS	For naming rule
8.	03/17	07 Delete { 檣纒触 \ 彪曉觸端 電彰 \ }	For ESD's request
9.	03/22	10 Add C21/C22/C23	For EMI's request
10.	03/22	31 Add C396/C397/C398/C399	For ESD's request
11.	03/22	21 Add C390 on +USB_VCCA	For ESD's request
12.	03/24	29 Delete net KS016 and KS017	W/O support 10 key
13.	03/24	07 Delete R127/R118/R119	For ESD's request
14.	03/24	31 Add C400/C40/C402	For ESD's request
15.	03/24	12 Add C332/C333	For ESD's request
16.	03/24	18 Add C287/C295	For ESD's request
17.	03/25	30 Change LPC debug port	For SW request
18.	03/28	18 Add C334	For ESD request
19.	03/28	12 Change C248 and C249 to 15PF	For RTC issue

REVISION C { 樗特鴿蹤E: 0.3 TO 1.0

NO	DATE	PA	DESCRIPTION	PURPOSE
1.	04/26	16	Add C521,C342,C335 and C336	For EMI request
2.	04/26	16	Delete Q56 and add R371	No need for AMD A13
3.	04/26	31	Add C403 and C414	For EMI request
4.	04/26	31	Change SW2 and SW3 to 0	For Debug use
5.	04/27	08	Change C201 to 330/9mohm))))))))	For Dynamic CPU_CORE_NB fail
6.	04/27	14	Delete 450 of U13	For Debug use
7.	04/27	10	Add C343/C344/C345/C346/C347/C348/C349/C350	For ESD request
8.	04/27	31	Add C426	For ESD request
9.	04/29	10	Change C343/C344/C345/C346/C347/C348/C349/C350 from 1u to 0.1u	For ESD request
10.	05/03	12)	Add C333 and C332	For ESD request
11.	05/03	13	Add C363	For ESD request

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